5G FPGA BASED SMART NIC

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ABSTRACT

Next generation communication relies on standard-ized protocols, heterogeneous architectures and advanced tech-nologies that are envisioned to bring ubiquitous and seamless connectivity. This evolution of communication will not only improve the performance of the existing networks, but will also enables various applications in other fields while integrating different heterogeneous systems. This massive scaling of mo-bile communication requires higher bandwidth to operate. 5G promises a robust solution by offering ultra-low latency and high bandwidth for data transmission. To provide individuals and companies with a real-time, social, and all connected ex-perience, an end-to-end coordinated architecture which is agile and intelligent has to be designed at each stage. As FPGA has the potential to be resource/power efficient, it can be used for building up constituents of 5G infrastructure. It can accelerate network performance without making a large investment in new hardware. Dynamic reconfigurability and in-field programming features of FPGAs compared to fixed function ASICs help in developing better wireless systems. This article presents various applications areas of FPGAs for the upcoming 5G network planning.

I. INTRODUCTION

The next generation of communications is beyond present-day Internet and is moving towards the Internet of Everything (IoE). 5G , a key pioneer in this will unleash an ecosystem for connecting billions of devices with optimal trade-off latency, cost and greater capacity. Fig.1(a) highlights certain salient features of 5G. It is estimated that, around 50 billion devices will be connected to the 5G network by 2020. So the network must be able to cope up with the diversified demands. Com-pared to today's 4G and 4.5G (LTE advanced), which is about speed improvement, the evolution of 5G focuses on connecting new IoT and critical communication use cases which require several performance enhancements [1]. IoT connections are characterized based on the volume of connection, data traffic, and energy consumption. For certain applications, such as self-driving cars, health services etc.. ultra-low latency communi-cations is a requirement and while for some other applications, devices operating on low power mode is an indeed requirement helping them to operate for longer duration without regular maintenance. On the other hand, there are several cloud-based applications for data analytics that require higher bandwidth and speed enhancement.

According to the International Telecommunication Union(ITU), 5G network services can be categorized as Enhanced Mobile Broadband (eMBB), Ultra-reliable and Low-latency Communications (uRLLC), and Massive Machine Type Communications (mMTC). eMBB focuses on services which require high bandwidth, such as high definition (HD) videos streaming, virtual reality (VR), augmented reality (AR) and web browsing. uRLLC aims at providing services to latency sensitive devices used in applications such as industrial automation, autonomous driving, remote surgery, and remote management. mMTC aims to meet the demands of the digital society where the connection density is high such as that for a smart city [2].

As shown in Fig.1(b), 5G is about distributed network architecture in which data from the core network is transmitted to the macro base stations through radio network controllers (RNC). 5G macro cells use “massive MIMO” (multiple inputs multiple outputs) antennas which benefit a number of users to connect simultaneously to the base network and provide higher throughput. As compared to the macro network, which has a wide coverage area, small cells can be used for shorter range operating in dense environments. Small cells operate in mm-Wave frequencies range and provide increased data capacity which improves the performance to the connected devices.

A. Technical Challenges in 5G infrastructure

Developing new type of communication systems depends on globally accepted standards which ensures interoperability and affordable cost for deployment of the system. Some technical challenges for meeting the demands of a 5G network are as follows:

1) Medium Access Control: In the case of dense deploy-ment of access points and user terminals, throughput of the system will reduce and latency would be high. So, there must be a proper protocol / algorithm for handling massive number of connected devices without affecting their performance.

2) Data-traffic management: Moving from traditional com-munication towards deploying machine-to-machine (M2M) communication will not only overload and congest the net-work, but will also pose a threat to the Radio access network (RAN).
3) Multi-Service network: 5G has to offer diversified ser-vices to heterogeneous networks and devices operating in different geographies. These devices may be having varied specification (i.e few might demand low latency, some may demand high bandwidth). So the transport network has to be intelligent enough to provide dynamic, user-centric and data-rich wireless services to various end devices satisfying to their specific need.

4) Power consumption: Reducing energy consumption for the services provided is specific to help end-user equipment have better battery life.
5) Communication, Navigation and Sensing: These ser-vices are highly dependent upon the radio spectrum allocated, as the transmission capacity depends on that.

The vision of 5G is strongly relying upon the hardware infrastructure. Hardware designs should be re-configurable

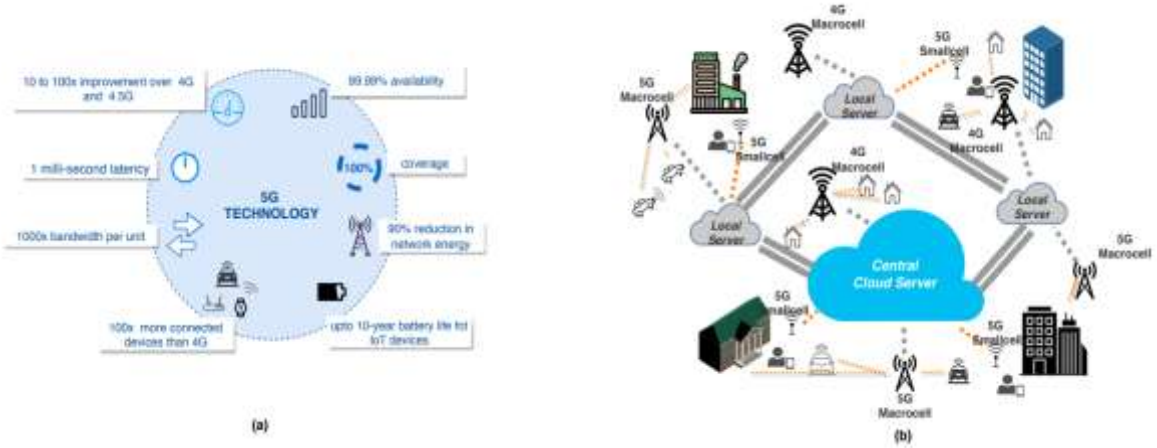

Fig. 1: a) Specification of 5G technology. b) 5G Network Architecture.

support multiple services, and to be easily upgradeable with new functionalitiesalong with efficient energy manage-ment and cost optimization. FPGAs (Field Programmable Gate Arrays) with the characteristics of Dynamic Partial Re-reconfigurability (DPR) and the ability to perform at higher frequencies make it convenient for designing various building blocks of the 5G architecture. Also, FPGAs have excellent advantages like hard real-time processing which helps in radio signal processing, parallelism which helps multiple kernel computation in the same FPGA and energy efficiency in case of fixed precision computations than GPUs . However there are a few challenges associated with the use of FPGA like they being costlier and having higher power consumption as compared to DSP and microcontrollers. Moreover they are difficult to program, and being less efficient in floating point computations. Also, ASICs (Application Specific Integrated Circuits) are more power efficient and perform better than FPGAs. FPGAs are only preferred when required volume of production is less, and time criticality to market is more. Note that various leading FPGA vendors like Xilinx and Altera are working hard to overcome these challenges and to improve FPGA design and performance. This work proposes different methods to solve the challenges in building the 5G communi-cation infrastructure using FPGAs. The main contributions of this article are as follows

1) We summarize different areas of 5G where FPGAs can play a key role.
2) The application of FPGA in realizing and improvising state of the art 5G technologies like Network slicing, MIMO, C-RAN virtualization etc. is discussed.
3) For each application, we describe technical details of how FPGA can be used in them, and also about current leading research efforts in those directions.

Please note that this is not a fully encompassing overview but focuses on certain crucial components of the future 5G systems.

II. APPLICATIONS OF FPGA IN 5G

5G is on the horizon of integrating IoT, machine-to-machine and machine-to-human communication along with the current communication technologies on the top of newer network in-frastructure such as cloud-based radio access network (RAN), software-defined network (SDN) and network function virtual-ization (NFV) etc.. Apart from Captial Expenditure (CAPEX), incurred during building preliminary infrastructure for 5G and annual maintenance, the Operational capital Expenditure (OPEX) has to be reduced so that the services can be provided at reduced rates. As the growth of users will substantially increase the number of base stations, this will lead to more power consumption and will put more burden on operational costs. Thus telecom operators are focusing towards minimizing operational costs and improving hardware and transmission efficiency. Also, issue of load imbalance in different regions at different times leads to the network resources being under-utilized.

The flexibility of FPGAs enables us to program various applications on on top it in different instances. The ability of the FPGA to re-configure itself dynamically enables us to change data transmission capacity along with switching between services as per the current requirement. All these abilities of FPGA are pushing leading FPGA manufacturers to invest more to make their hardware more capable of dealing with growing communication technologies. As FPGAs are performing well in signal processing, giving faster output and higher throughput, they can be used for signal filtering in telecommunication.

Xilinx is providing support for solving performance, capac-ity and connectivity challenges. It is providing FPGAs which are embedded with software programmability, multi-band, and multi-standard hardware optimization along with hardware level security. Xilinx has developed Zynq MPSoC, RFSoC, Ultrascale+ FPGAs and software platforms such as Vivado High-level synthesis, SDSoC and SDAccel for customers to build their applications [3]. Similarly, Intel has designed FPGA based accelerators for handling high-speed data transmission and greater bandwidth for virtualized workloads. There are various building blocks of 5G architecture which can be designed with the help of FPGAs for better performance. In this paper we discuss four such major applications namely, FPGA based accelerator for C-RAN, Netwrok slicing using Network function Virtualization (NFV), Characterization of Massive MIMO and Cognitive radio framework.

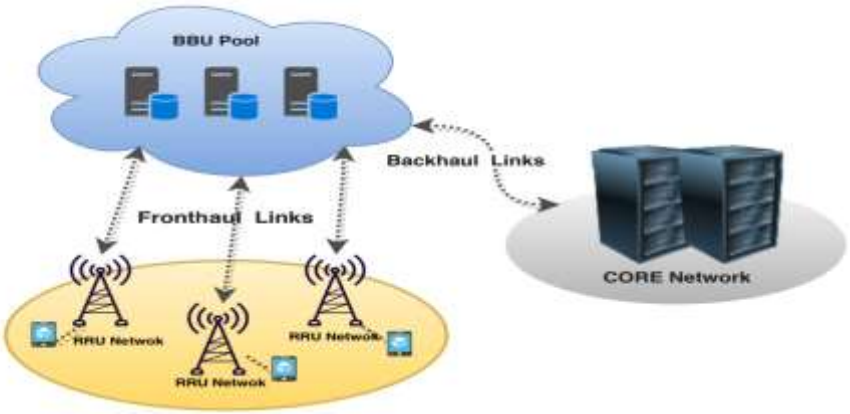

Fig. 2: Centralized RAN Architecture.

III. FPGA BASED SYSTEM DESIGN FOR C-RAN

Radio Access Network is designed to communicate between base stations and end users. C-RAN (Cloud Radio Access Network) is a novel architecture meant for centralized and cloud-based processing, where the Base Band Unit (BBU) are relocated to a centralized pool termed as BBU pool. It enables collaborative radio network, real-time workload virtualization and large scale deployment. These BBU pools are connected to the network stations through the high-speed optical fibre and maximize the distance between macro to small cells. The C-RAN architecture can be perceived as a cloud-computing environment where the baseband and channel processing is virtualized and shared among the operators in the baseband pool, which leads to better traffic handling and maximum utilization of resources. It is built on interfacing cards and hardware which creates links between base stations and optical fibre network.

Apart from easier deployability and scalability, the cost-effectiveness and manageable solution towards a huge user base will make it a reliable infrastructure component for 5G. Fig.2 highlights that C-RAN architecture is built upon three key components: The Base-band Unit (BBU) Pool, Remote Radio Unit (RRU) network and Transport network [4].

The BBU pool: The BBU pool is located at a centralized site, functioning as a data centre. It holds a number of baseband nodes which are capable of performing complex computations and storing huge data. It has the ability to dynamically interconnect within the nodes or work individ-ually as per the network needs. The communication among the units happens on a larger bandwidth, and lower latency. After processing, it allocates resources to the RRUs as per the network demand.

RRU network: It is a traditional wireless network which connects wireless devices to the access points.

Transport network: It is also termed as Fronthaul network. It is a communication layer between the BBU and the RRUs which provides a high bandwidth channel for handling

multi-ple RRU networks. It can be optical fibre based linking capable of transferring high bandwidth and with a faster rate, but it adds on more cost. On the other hand, we can have cellular communication at an mm-wave level which is much cheaper than optical fibre. 3

There are various challenges in deploying C-RAN architecture, some of those with possible solutions are listed below:

A. Cooperation in BBUs

The BBUs in the same pool should cooperate with each other to share the computing data and should schedule them as per user requirement. But such cooperation is not defined and that introduces challenges in ensuring low latency, high bandwidth communication among the BBUs and also affects the user privacy.

FPGA based Solution: High performance logic in FPGA can be used to reduce latency of interfacing among the base band units. At high-capacity base stations, integrated block ram can be used for switching among the BBUs.

B. Virtualization

Virtualization techniques promote the BBUs to share the resources autonomously and increase the lifecycle of RAN functions. But the dynamic change of loads and real-time processing requires a robust virtualization technique which is different from current IT virtualization techniques such as virtual multimedia IP subsystem, virtual customer premise equipment etc. where multiple operating systems and appli-cations run on the same server at same time in a single physical machine which includes network, storage, and com-puting resources. In the context of C-RAN, virtualization is done at the BBU pool level, where each BBU acts as a virtual node which is implemented on the virtual machine and communicates through virtual links. C-RAN virtualization requires sophisticated switches and routers, which are aimed to replace the software implementation on high volume servers, and storage units in case of IT clouds, to reduce overall cost and power. Hence, meeting low latency and higher bandwidth requirements for centralization of RAN functions is raising a critical challenge for realizing virtualization in current C-RAN practice [5].

FPGA based solution: The ability of FPGA to modify its operation at run-time with partition safe mode, enables it as a shared compute resource in C-RAN. FPGAs can run multiple applications by virtualizing compute resources and also offers protection through isolation of applications from each other.

C. Multi-Connectivity

As dual connectivity feature in LTE helps devices access base stations on different frequencies (e.g. macro and small cells). Similarly multinetwork connectivity in 5G over multi-mode base stations such as GSM, LTE, UMTS and WiFi enhances peak throughput of the devices. But deploying a multi-mode base station increases the capital cost.

FPGA based solution: Multi-connectivity can be realized by using Software Defined Network (SDN) and Software De-fined Radio(SDR), as they offer cheaper approach than a multi-mode base station. SDN's and SDR's are designed with an approach of integrating software and hardware infrastructure, where software can perform controlling and hardware as a compute resource. The ability of partial reconfiguration in FPGAs, enable it to handle multiple operations and acts as a hardware accelerator for complex computation. This solution is discussed in detail as follows.

Software Defined Approach towards the multi-connectivity issue: As the implementation of the multi-mode base stations for building a multi-network system is a costly approach, so we can realize the same using SDN's and SDR's. SDR's can be used for allocation of radio (spectrum) resources to multi users, where as SDN's can be used for dynamic network re-configuration. Integrating both, SDR and SDN can adhere to changes in frequency and communication pro-tocols through software reconfiguration at lower costs. But the challenge of handling high bandwidth and low latency communication requirements puts limitation on software-based solutions. This is because the SDR base stations also need to perform computation-intensive tasks at high speed. To deal with such complex tasks, Hardware accelerators can be used along with software technologies such as turbo decoders, FFT etc. Hardware accelerators can improve performance and are faster as compared to software-based processing. Through vir-tualization, the utilization of hardware resources such as FPGA and GPUs can be improved by replacing the small physical servers with larger ones. The SDR signal processing can be performed using FPGA and Xen platform based hardware accelerator [6].

System has structure as in Fig.3(a), which includes a SDR platform and a custom hardware accelerator. FPGAs are very good accelerators as compared to GPUs because their latency are far less than the GPUs. In FPGA, algorithms are embedded into the hardware and thus processing speed is far better than a software-based GPU process. This is because software processes have to share processing resource (OS etc.) which is not the case with the hardware based solution. Xen hypervisor can be used which can enable multiple OS to run on a single computer and also provides a special API to access the hardware. It also supports para-virtualization which can reduce performance loss. Some SDR platforms based on DSPs and FPGAs can be used to minimize power consumption and improve the processing density of the baseband units.

Multi-mode base stations need high bandwidth and a cost effective resource allocation technique to efficiently implement multi-network communication. These base stations can be run on hardware accelerators for faster signal processing. A Turbo decoder accelerator can perform better SDR signal processing with high bandwidth, and also sort out timing constraints.The Turbo decoder accelerator can be designed using Xen para-virtualization environment and FPGA as an accelerator which can enhance the performance of C-RAN based signal processing [7]. The SDR base stations can deploy FPGAs to accelerate the decoding process which will reduce the overall signal processing time effectively.

Turbo-Decoder design and Operation over FPGA: The system consists of customized hardware as accelerator and a virtualization environment which can support multiple guest OS to run simultaneously, individually corresponding to singular Virtualization Base station. The accelerator architecture can be implemented on FPGA using Verilog Hardware defined language and some predefined IP cores on the Xilinx synthesis tool. The host OS will consist backend driver for PCIe and Xen environment and the Guest Os will hold the frontend drivers which will be used for transmitting data between SDR base stations.

The decoder can be implemented along with encoder to improve the transmission efficiency of digital communication over the noisy data channel. Turbo coding is a very powerful error correction technique which can be implemented to detect and correct the errors when the communication channel is noisy. The turbo decoder iterates many times to provide the decoding result. To reduce the latency in decoding, FPGAs can be a better alternative over traditional CPUs.The high clocking frequency and the parallel pool base processing can speed up the decoding process.

As shown in Fig.3(b) Turbo decoder architecture consists of three layers: Top layer, Control layer and Decoder layer.

Top Layer consists of the data and signal transmission drivers such as the PCIe hardware interface and DMA con-troller. The data and control signal can be transmitted between the PCIe driver of FPGA and the server driver which is part of the top layer.

Control Layer acts as an intermediate layer which passes the data and control parameters(such as Block size, reset signal etc) between the PCIe hardware driver and the decoder and vice-versa.

Decoder Layer can be implemented using the IP core for turbo decoder under 3GPP LTE decoder core. In this layer, data caching can be done using a FIFO and also asynchronous clocks can be isolated from DMA and decoder. When data and control signals are received in the decoder layer, it is written into RX FIFO which also masks the invalid data. After processing the data in the decoder core, it is sent to the TX FIFO. Then the control layer reads the data from the TX FIFO after reading its status.

After designing and implementing the turbo-decoder on FPGA it can be simulated using various synthesis tools such as Xilinx ISE, Vivado HLS and Modelsim etc. By designing a scheduling algorithm and pushing it into accelerators, we can achieve multitasking and resource sharing among the accelerators holding VMs, individually.

IV. NETWORK SLICING USING NETWORK FUNCTION VIRTUALIZATION OVER FPGA

Network-slicing is a typical virtual architecture belongs to the software-defined network (SDN) and Network function virtualization (NFV) family which will be designed through

logical partitioning of physical resources. Slicing introduces custom tailoring of the network which enables the operators to customize their services as per consumer demand [8]. Fig.4(a) highlights the assignment of individual slices for different ser-vices as per the users network requirements. Network slicing will offer resource sharing ability to the service providers through which they can improve the quality of service. A single physical network can be sliced up logically through a software-based approach into multiple networks such as Ultra bandwidth service for mobile broadband, Ultra-low latency and high reliability for transportation, no reservation for machine type communication etc. Also, the software-based techniques can add up more slices dynamically and also share the unused slices with others. As the services can configure itself as on demand, so the overall operational expense can be reduced.

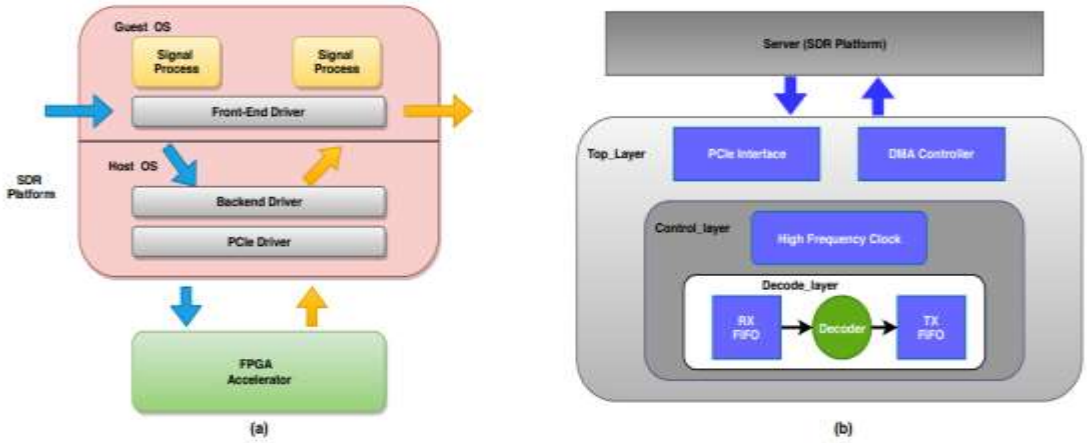

Fig. 3: a) System Design. b) Turbo-Decoder Architect.

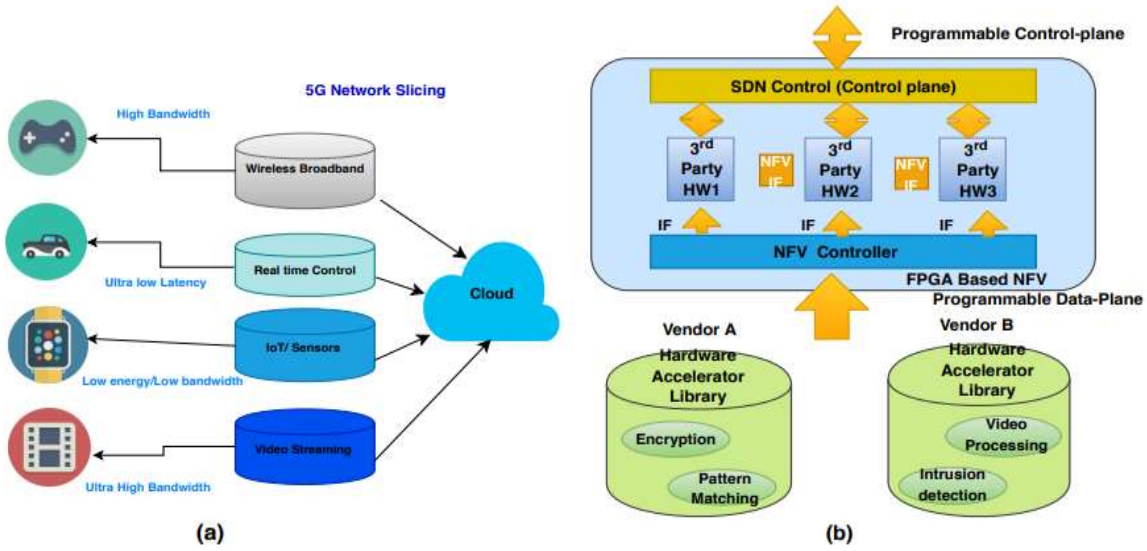

Fig. 4: a) Network Slicing Architecture. b) FPGA based NFV.

Challenges in Network-Slicing: As network slicing is a promising solution towards maximization of network resource utilization, however various challenges are to be addressed for building such infrastructure. The various challenges that are faced to deploy a software-defined network slicing environ-ment are listed below

Isolation of Service: This is a challenging factor in network slicing because the data packets for different services shared within a single resource must be properly isolated so that individual service performance is not affected.

RAN re-designing: This is required so that all the slices can be accessed through various mediums such as macrocell, microcell and wifi. These mediums must work coherently in-order to share network slices. Even in some medium, different
users need different slices varying with different class of QoS. This is a complex task and needs ultra-low latency synchronization between the mediums.

Assuring Services: If there are multiple services which have the same sort of network requirement, then it becomes difficult to prioritize the services and to schedule the slices according to that. Network slicing creates challenges for each slice to meet its endpoint demand in the network.
Slicing Management: The operator needs to manage the network slices so that each slice can adhere to the key performance metrics and service level agreements [9]. For different heterogeneous systems, interoperability issue must be overcome if a single slice is being used by different vendors.

All the above issues can be addressed using Network Func-tion Virtualization (NFV), and thus we discuss this solution in detail and how FPGA can help in implementing the same.

End to end Network slicing through Network Func-tion Virtualization (NFV): Upcoming section briefly dis-cuss about the benefits of Network Function Virtualization (NFV), in overcoming above mentioned challenges. 5G end-to-end network slicing provides extreme flexibility to provide various services over a single channel. Through software programmability, we can logically define the application of slices from user equipment level to cloud servers. Through network virtualization software can provide us with more programmable capability and flexibility in terms of creating logical virtual networks. Furthermore, through virtualization we can effectively share resources among slices. A software-defined controller can perform orchestration process which can bring together and coordinate diverse services to work coherently over slicing environment. By integrating virtualization and orchestration in a system, isolation among the slices can be achieved effectively, as isolation plays an important role in providing more privacy, performance enhancement and managing the individual network more effectively.

Network function virtualization reduces the time to establish a new network by downloading the network function onto the hardware and also increases the life cycle management of the network slices. Network function virtualization infrastructure is built upon adjoining

resources used to host and connect the network functions. Network management and orchestration system can perform general networking tasks, coordinate and automate the tasks. FPGA as a customizable hardware, can be prototyped and introduced into the market within a short span of time. So the network function virtualization over FPGA can reduce the expenditure of purchasing huge hardware resources. An SDN controller can be introduced to centralize the control plane which will manage the connectivity among components.

Flexible service provisioning is one of the motives of Virtualization of network function, which can be achieved by using FPGA as the main hardware. Faster deployment time using FPGA reduces time to provide newer services efficiently. As as shown in Fig.4(b), FPGAs can be equipped with various hardware components as per third party application requirements. Each FPGA can have different capabilities as per the service demand from end application. This will encourages the innovation and also opens market for vendors in this emerging domain, which can work coherently within the same ecosystem. A competitive market will be built for the FPGA vendors and IP block providers. Multiple vendors can provide hardware which can be used as accelerators for multiple application such as, Vendor A provides encryption module whereas Vendor B provides video compression module [10].

In application areas where we need to satisfy a high degree of flexibility and performance, FPGA based NFV can be a promising platform. It offers similar flexibility, but better throughput than GPUs.

V. FPGA CHARACTERIZING MASSIVE MIMO

Massive Multi Input Multi Output (MIMO) system can improve the throughput, network capacity and reliability over the traditional single input single output (SISO) system. MIMO has been introduced two decades back and has been used for 4G LTE service. As 5G will bring a revolution by connecting large number devices together, a robust networking system MIMO system has to be modified to accommodate in this complex ecosystem. Massive MIMO such as Multi-User MIMO (MU-MIMO) delivers significant performance improvement over the busy network traffic. MIMO includes

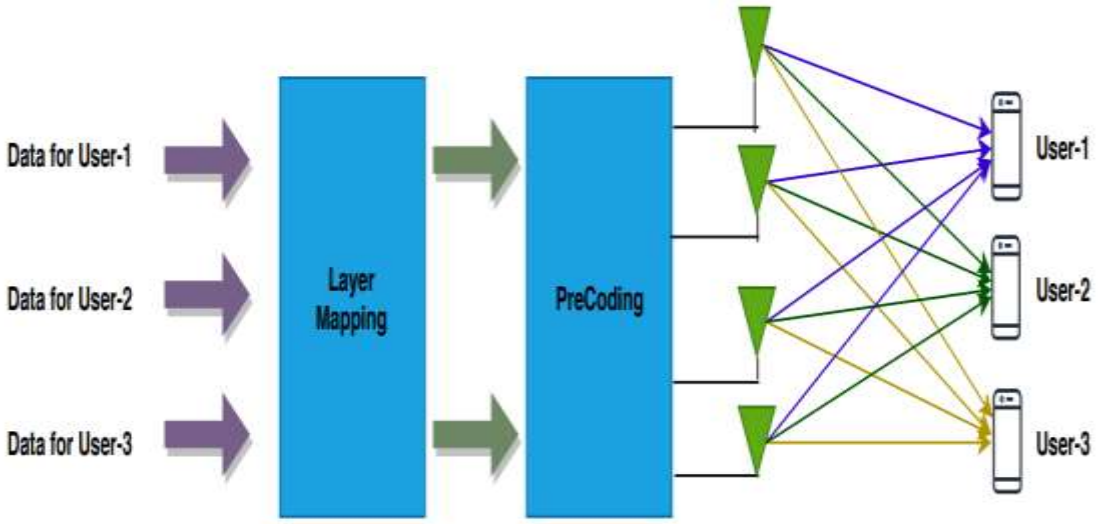

Fig. **5: Massive MIMO network architecture**.

multiple antennas at the base stations and access points; both at the transmitting and receiving end by separating independent wireless channels to provide rich communication over a multi-path environment to serve multiple clients simultaneously. In massive MIMO the base stations are equipped with a large number of antennas (e.g 100 or more). The architecture of massive MIMO is shown in Fig. 5, which shows multi-user input and output through multiple transmitting(Tx) antennas and Receiving (Rx) antennas while pre-processing the user data at the single BS. MU-MIMO serves the application for all single antenna users and also through multiplexing, the gain can be shared among its users. Installing massive MIMO can enhance the channel capacity and provide better signal strength for individual users. The massive MIMO is made up of an array of antennas which consume very low power and also reduces the complexity of hardware which is a concerning factor for base stations. It also provides the flexibility of sharing the resources to other antennas when anyone antenna fails.

Challenges in MIMO deployment: Apart from numerous benefits of a MIMO system, there are some issues in deploying such a large system and those needs to be addressed. The following are some of those issues.

A. Wireless Propagation Environment

Every node in MU-MIMO can serve multiple users si-multaneously. So accurate measurement of the propagation channel for each user needs to be done at real-time. Statistical analysis of the recent measurements of the channels with optimum accuracy is challenging and the performance impact of inaccurate information can be severe.

FPGA based local processing of data: Serving multi-ple users in MU-MIMO requires accurate knowledge of the communication channel. But collecting information about the channel in real-time is challenging and it also impacts the performance of the system. To solve this issue, an integrated device platform is being proposed by Mango communication and Rice University, which uses FPGA stack to process raw channel data between the

antennas to characterize massive MIMO. The data gathered by each antenna is condensed as per individual client channel characteristics.

The Wireless Open-Access Research Platform (WARP) is a programmable wireless platform which combines high-performance hardware along with open source repository of the reference design [11]. WARP is designed for real-time prototyping of wireless designs. The FPGAs in WARP node in Argos array of FPGAs has huge processing capability which can perform real-time processing of data locally and reduce the burden on the upstream processor. This real-time processing of channel data in the submillisecond range allows accurate characterization of the antenna and enhance the performance per client. FPGA is capable of converting low-speed signal processing to high speed, which helps in real-time processing of data. Modern FPGAs feature 300-400 MHz parallel pro-cessing ability.

B. Standardization of Technology

For the next phase of development and verification, a proof-of-concept platform i.e testbed needs to be designed to operate Masssive MIMO under real life conditions. Testbeds can be helpful in overall understanding of the system and can mature the technology for standardization [12]. But designing a testbed with complex computation capability and real time operation has been challenging with the existing hardware resources.

MIMO testbed over an FPGA: Finding out the channel properties and the optimal transmission technology of the MIMO system is a subject that is being researched by re-searchers worldwide. One of the concerning areas is signal propagation scheme, which can be implemented over a testbed before actually putting into operation. Handling increased data over multiple channels in multiple antenna system of MIMO over the testbed poses a challenge in designing such processor. Specific processor that can handle parallel processing at a faster rate are preferred. FPGAs are capable of handling increased data transmitted through multiple antennas due to its parallel processing capability. FPGAs are advanced signal processing devices which can process the transmitted and received data over the virtual parallel pool. The high-speed analogue to digital (ADC) and Digital to analogue (DAC) converter ports can be used for faster delivery of data to the output circuitry.

VI. COGNITIVE RADIO FRAMEWORK FOR 5G

The potential increase in the number of users in a mobile network and the requirement of high data rates pushes 5G to work within a mixed ecosystem of micro and macrocells. Further, the standalone base stations will be replaced by a centralized system as per availability of high bandwidth backhaul network. So adequate amount of spectrum allocation is required to be performed efficiently.

The radio-frequency spectrum is part of nature, so the licensing and regulation of the spectrum is handled by the gov-ernment. However, fixed spectrum allocation by government bodies leads to underutilization of resource when a certain spectrum range is idle. So

accessing this under-utilized spec-trum is a challenging problem than the spectrum scarcity itself, since failing to utilize existing spectrum. Here, Cognitive Radio (CR) has the ability to identify the under-utilization of spectrum and to allocate the under-utilized spectrum to the secondary users that are not being served. This can also reduce the burden on single network thus providing ubiquitous high-speed communication channel.

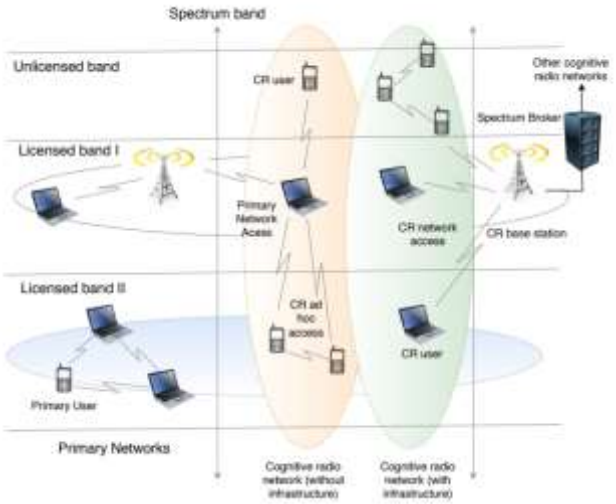

Fig. 6: Cognitive Radio(CR) framework for 5G.

CR empowers progressively unique and adaptable spectrum access in which the secondary system can get the spectrum
resources from the primary system. Fig.6 highlights the cogni-tive radio framework that ensures network access among users of licensed and unlicensed spectrum band. In CR network access, CR users communicate through the CR base-station. When there is a lack of CR network infrastructure, CR users share resources through ad-hoc connections in both licensed and unlicensed spectrum bands. In CR network, the secondary system senses the white spaces in frequency spectrum, time and potential geographic area that stay underutilized by the primary system and CR allocates those white spaces to the secondary system without interfering the performance of pri-mary users. Through spectrum sensing and maintaining the overall geographic database, the spectral white spaces can be found .

CR is a complex computational networking system which performs various digital signal processing algorithm on various platforms. The general purpose processors provide us with greater flexibility but don’t provide better performance. How-ever the application specific integrated circuits provide great performance but lack flexibility. FPGAs are the best option as they provide both flexibility and performance along with low power consumption.

Cognitive Radio platform using FPGA: Various researchers have worked on developing a cognitive wireless platform using FPGA as hardware. A cognitive radio known as Agile radio is developed by Kansas University researchers which embed Linux, FPGA, RF front-end and antennas to work on dynamic spectrum allocation [13]. WINLAB at Rutgers University has also developed a network-oriented cognitive radio which focuses on multi-band frequency

operation. It uses an embedded OS for controlling the operation along with Xilinx FPGA for processing baseband signals [14].

At Trinity College, a cognitive radio platform is developed on the basics of programmability of the software-defined network. The Implementing Radio in Software(IRIS) provides a highly reconfigurable software radio platform [15]. It is made up of various digital signal processing components which can perform various distinctive tasks. Linux has to be ported into the Xilinx FPGA to control the operations. The DSP operations can be implemented in the logic fabric of FPGA as the hardware level implementation is always faster than the software-defined operation. The static part of the FPGA i.e the Programming Subsytem (PS) of the FPGA is used to run the Linux OS. A composer generates the bitstreams for FPGA to reconfigure and implement various radio component and also directs some other radio component implementation on the PowerPC processor [15].

VII. CONCLUSION

This article gives an overview of 5G technology and integra-tion of various hardware and software-defined technologies to meet the requirement of future mobile communication. Also, it explains how FPGA can be used to create various building blocks of 5G infrastructure. The invention of hybrid computing platforms, such as the FPGA-based hardware acceleration approach, shows promise for the implementation of standalone energy efficient NFV and C-RAN architectures. An efficient real time signal processing architecture can be designed to charecterize the massive MIMO. Cognitive Radio provides broad range of applications to run while supporting high data traffic. It's performance can be enhanced by using FPGAs to orchestrate and combine the operations of small cells along with micro and macro cells, so as to efficiently allocate the spectrum to avoid under-utilization of resources.

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