Comparative Analysis of 4-bit and 1-bit Full Adder using CMOS and Transmission Gate Logic Styles for various Technology Nodes

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Abstract:

This study presents a comprehensive comparison of 4-bit full adder cells and 1-bit full adders implemented using two different logic styles: Complementary MOS (CMOS) and Transmission Gate (TG). Simulations are conducted for 1-bit full adders at three technology nodes, namely, 180nm, 45nm, and 32nm. The performance and efficiency of both 4-bit and 1-bit full adder designs are analyzed by considering various parameters such as average power consumption, supply voltage, and transistor count. The results indicate that, within a given logic style, as the technology node decreases, the average power consumption decreases while the area also decreases, with a constant supply voltage of 15V. Furthermore, the analysis reveals that the transmission gate-based 4-bit full adder and 1-bit full adder consume less power compared to the conventional CMOS design.

Keywords: Full adder, CMOS, Transmission Gate, technology scaling, average power consumption, supply voltage, transistor count, power efficiency.

I. INTRODUCTION

Digital arithmetic circuits are integral in a wide range of applications, including microprocessors and digital signal processors, as they are responsible for performing fundamental arithmetic operations. Within these circuits, full adders hold great significance and have garnered significant attention due to their potential for optimization and performance improvement. This study focuses on comparing the performance and efficiency of 4-bit and 1-bit full adders using two distinct logic styles: Complementary MOS (CMOS) and Transmission Gate (TG). The objective is to determine the most efficient logic style between CMOS and TG for both 1-bit and 4-bit full adder circuits.

II. FULL ADDER DESIGN

a. This study presents the designs of 4-bit and 1-bit full adders, along with details of their architectures and circuit implementations. Two logic styles, CMOS, and TG, are utilized to realize these full adders. The designs are specifically targeted at achieving improved performance and efficiency. Designing a 4-bit full adder involves combining four 1-bit full adders to create a circuit that can perform addition on four binary inputs and produce a 4-bit sum output and a carry output. Here is a high-level overview of the 4-bit full adder design:

b. 1-bit Full Adder:

Initially, we need to design a 1-bit full adder. A 1-bit full adder takes three inputs: A, B, and Carry-in (Cin), and produces two outputs: Sum (S) and Carry (Cout). The truth table for a 1-bit full adder is as follows:

Table 1: Truth table of a full adder

A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The 1-bit full adder can be implemented using logic gates such as AND, OR, and XOR gates.

c. 4-bit Full Adder

Once we have the 1-bit full adder design, we then construct the 4-bit full adder by combining four instances of the 1-bit full adder. The inputs to the 4-bit full adder are four sets of A and B inputs (A3-A0 and B3-B0) representing the four bits to be added, and a Carry-in (Cin) input. The carry output of each 1-bit full adder is connected to the carry input of the next full adder in the sequence. The sum outputs of the four 1-bit full adders form the 4-bit sum output (S3-S0), and the carry output of the final full adder becomes the Carry-out (Cout). The 4-bit full adder can be implemented by cascading the 1-bit full adders and appropriately connecting the carry inputs and outputs.

III. Circuit Description:

A. Complementary MOS logic style (CMOS):

CMOS design is a methodology for designing digital logic circuits using complementary metal-oxide-semiconductor technology. CMOS design uses both n-channel MOS (NMOS) and p-channel MOS (PMOS) transistors to implement logic functions. NMOS transistors act as switches when the input is high (logic 1), while PMOS transistors act as switches when the input is low (logic 0). CMOS gates consist of a pull-up network (PMOS transistors in series) and a pull-down network (NMOS transistors in parallel). CMOS gates can implement various logic functions like AND, OR, NOT, XOR, etc. CMOS design offers low power consumption because power is only consumed during switching transitions. CMOS technology can be scaled down to smaller feature sizes, leading to increased circuit density and higher performance. CMOS design is widely used in microprocessors, memory chips, and digital systems. Designers use computer-aided design (CAD) tools and simulation software for CMOS circuit design, analysis, and optimization.

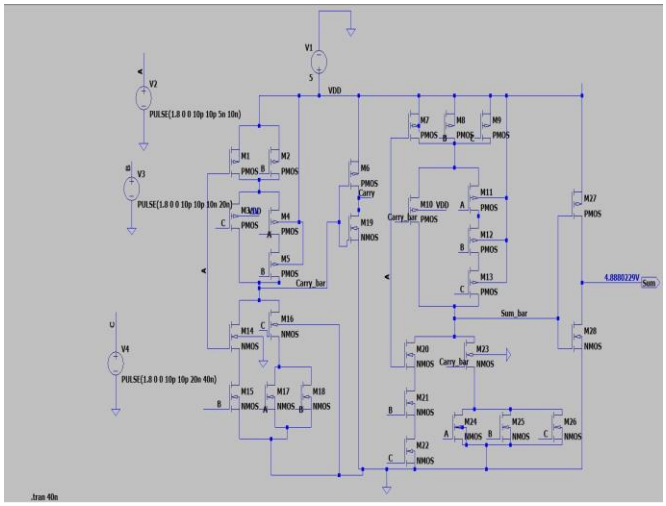


Fig 1. 1-bit full adder circuit using CMOS technology

4-bit full adder using CMOS, we can implement each stage of the full adder using CMOS logic gates. Here is a representation of the 4-bit full adder using CMOS gates:

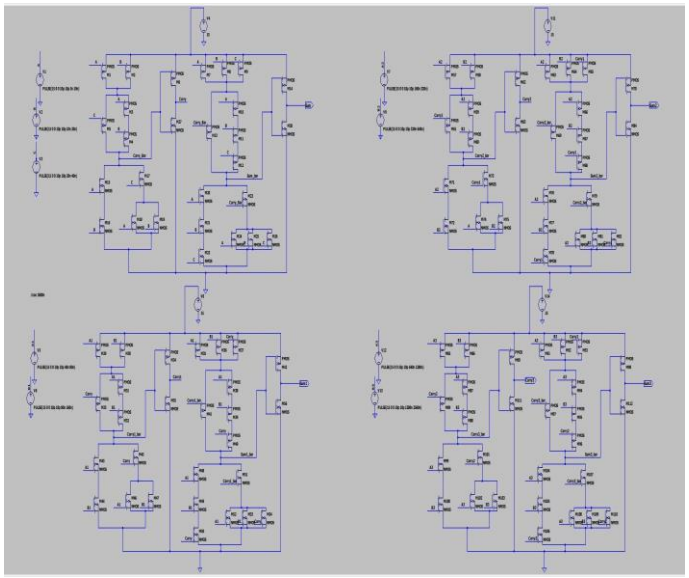


Fig 2. 4-bit full adder circuit using CMOS

In Figure 2. Each stage of the 4-bit full adder consists of CMOS logic gates. The inputs (A3-A0, B3-B0, and C) are connected to the appropriate CMOS gates to perform the addition. The carry outputs (Carry Out 3-0) are the carry outputs for each stage, and the sum outputs (Out 3-0) are the results of the addition.

B. Transmission Gate logic style (TG):

The transmission gate circuit typically consists of n-channel and p-channel MOSFETs connected in parallel. When the control signal is applied to the gate terminals, both the n-channel and p-channel transistors turn on or off simultaneously. In the on state, the transmission gate provides a low-resistance path between the input and output, allowing the signal to pass through with minimal voltage drop. In the off state, the transmission gate acts as an open circuit, blocking the signal flow.

The advantage of using transmission gates in a circuit is their ability to provide bidirectional signal flow without the need for additional circuitry. This makes them useful for applications such as signal multiplexing, bidirectional data transfer, and level shifting. By utilizing transmission gates, the circuit

achieves high-speed operation and minimizes power dissipation. This makes transmission gates suitable for applications where both speed and power efficiency are important factors to consider.

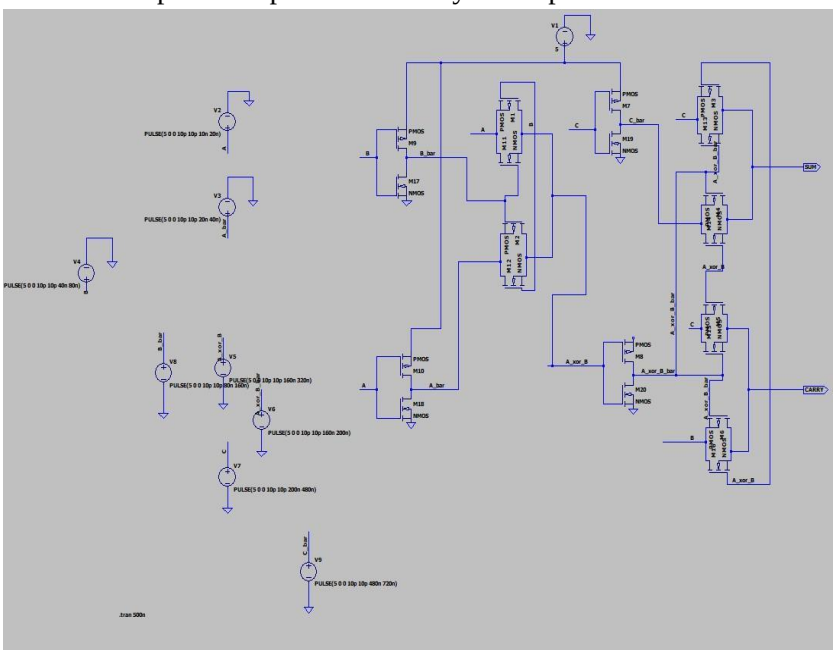


Fig 3. 1bit Full adder circuit using transmission gate

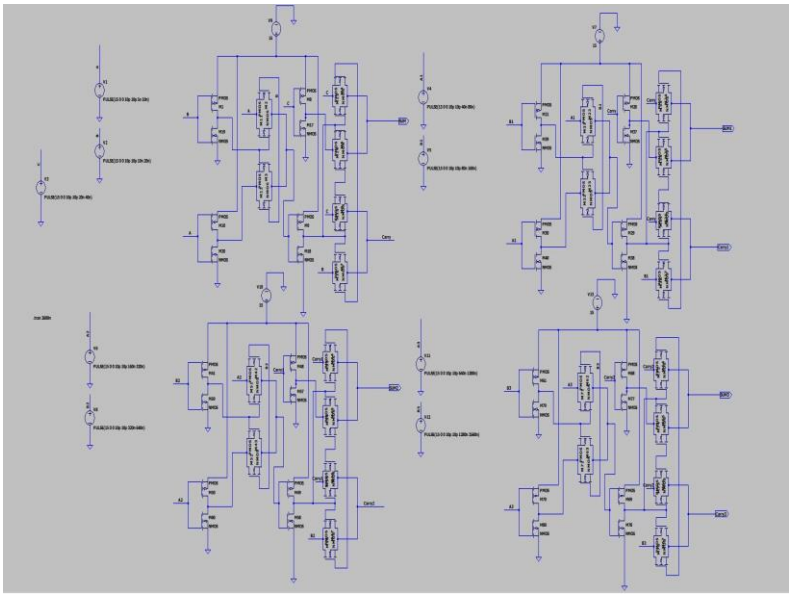


Fig 4. 4bit Full adder circuit using transmission gate

In Figure 4. Represent that 4-bit full adder circuit using Transmission Gate logic, each stage of the adder consists of Transmission Gates (TGs) for implementing the logic functions. The inputs (A3-A, B3-B) are connected to the TGs to allow bidirectional signal flow. The carry-in (C) is directly connected to the TGs. The carry outputs (Carry- Carry3) represent the carry-out signals for each stage, while the sum outputs (Sum 3-Sum) represent the results of the addition.

IV. Results and Discussion:

We first implemented in gate level using Vivado software. The RTL schematic of 4-bit Full adder circuit have been presented in fig. (5).

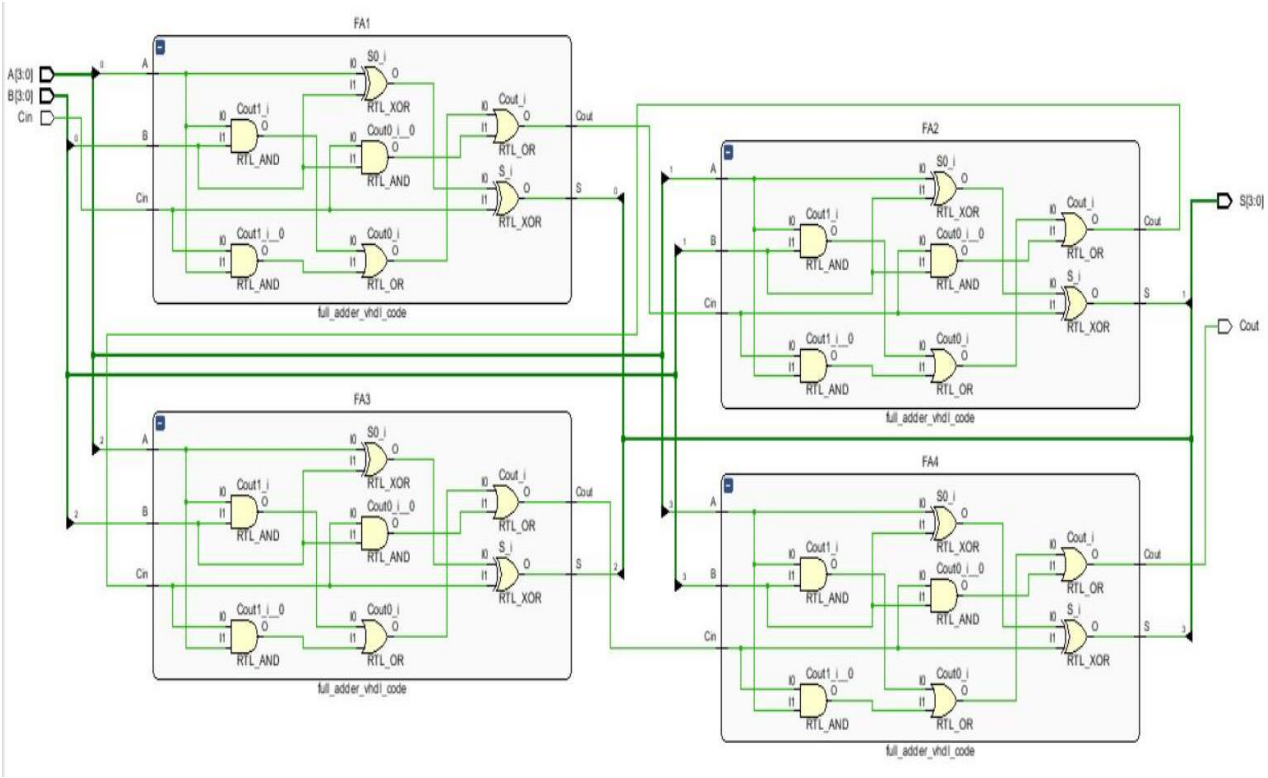


Fig 5. RTL Schematic diagram of 4- bit Full Adder circuit

The RTL schematic of a 4-fit full adder can be seen in figure 4, showing the basic gates in the circuit. The various inputs and outputs, data path lines can also be seen.

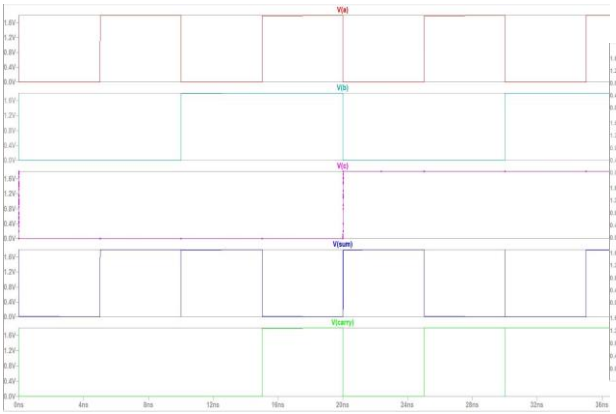


Fig 6. 180nm technology of 1bit Full Adder using CMOS technology

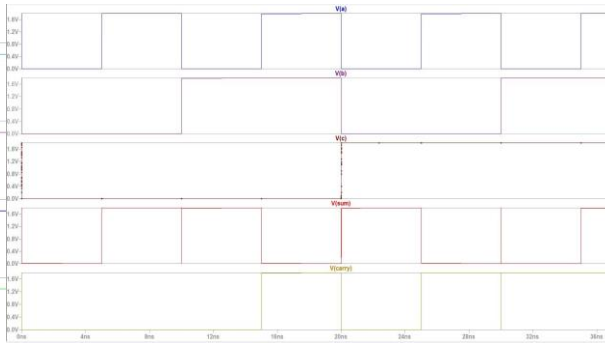


Fig 7. 45nm technology of 1bit Full Adder using CMOS technology

Figure 6 shows the 180nm technology of 1bit Full Adder using CMOS technology and figure 7 shows the simulation result using 45nm technology of 1bit Full Adder using CMOS technology.

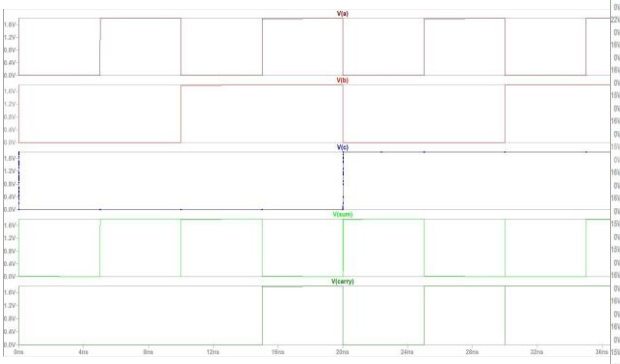


Fig 8. 32nm technology of 1bit Full Adder using CMOS technology

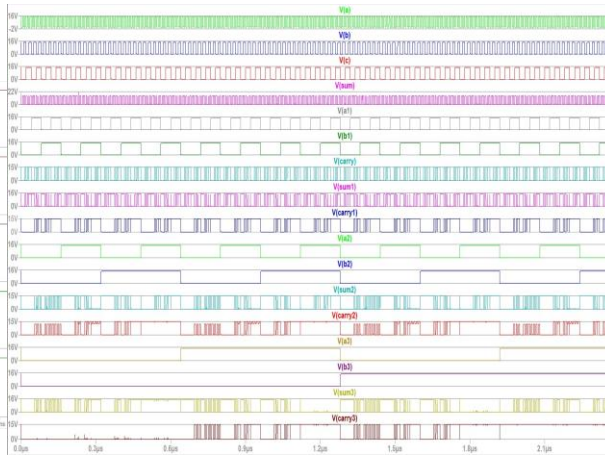


Fig 9. 180nm technology of 4bit Full Adder using CMOS technology

Like the above simulation results, figure 8 and 9 shows the 32nm technology of 1bit Full Adder using CMOS technology and 180nm technology of 4bit Full Adder using CMOS technology respectively.

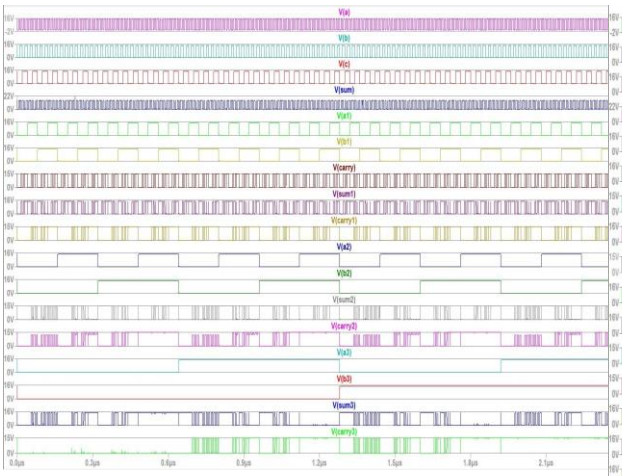


Fig 10. 45nm technology of 4bit Full Adder using CMOS technology

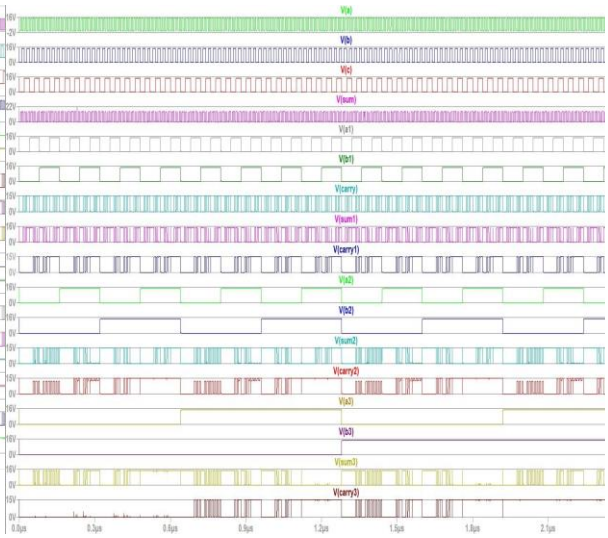


Fig 11. 32nm technology of 4bit Full Adder using CMOS technology

Figure 10 show the simulation results of 45nm technology of 4bit Full Adder using CMOS technology and figure 11 shows the result of 32nm technology of 4bit Full Adder using CMOS technology.

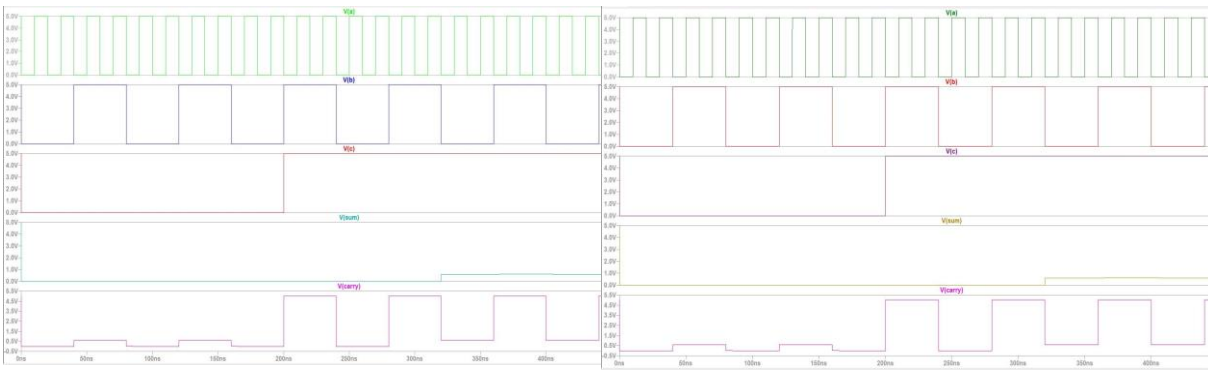


Fig 12. 180nm of 1-bit Full adder using transmission gate

Fig 13. 45nm of 1-bit Full adder using transmission gate

Figure 12 show the simulation results of 45nm technology of 4bit Full Adder using CMOS technology and figure 13 shows the result of 32nm technology of 4bit Full Adder using CMOS technology.

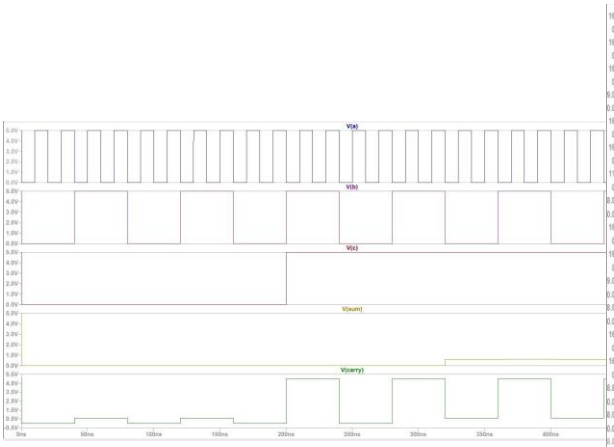
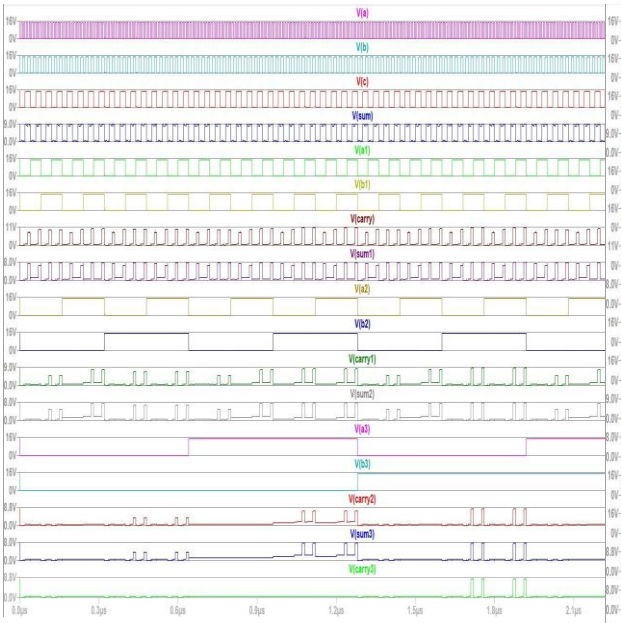


Fig 14. 32nm of 1-bit Full adder using transmission gate

Fig 15. 180nm of 4bit Full adder using transmission gate



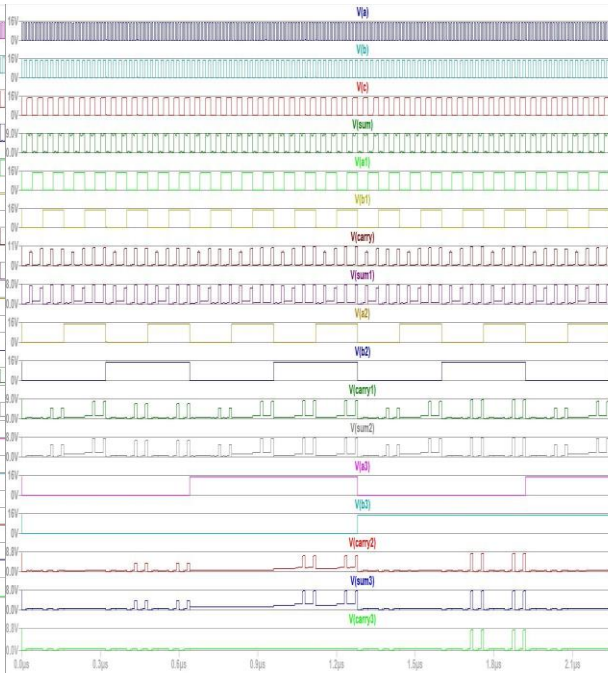


Fig 16. 45nm of 4bit Full adder using transmission gate

Fig 17. 32nm of 4bit Full adder using transmission gate

V. Performance Analysis

Table 2: Performance parameters of 4-bit Full adder of CMOS & Transmission gate technology

Parameters	**4-Bit full adder using CMOS logic style**			**4-Bit full adder using Transmission Gate logic Style**		
Technology (nm)	180	45	32	180	45	32
Transistors Count	112	112	112	80	80	80

Average power (µW)	0.65	0.15	0.10	0.45	0.11	0.07
Delays (µs)	0.0000147	0.0000147	0.0000147	0.0000063	0.0000063	0.0000063

Based on Table 1 and 2, the comparative analysis of the 4-bit full adder circuit using CMOS and Transmission Gate (TG) can be summarized as follows:

A. Performance Analysis:

The average power consumption of the CMOS 4-bit full adder is higher compared to the Transmission Gate implementation.

B. CMOS Technology Analysis:

i. When comparing different technology nodes (180nm to 32nm) while keeping the voltage constant, the transistor count remains the same.

ii. As the technology decreases, the average power consumption of the CMOS 4-bit full adder decreases from 0.65µW to 0.10µW.

iii. The minimum power consumption is observed to be 0.10µW for the 32nm technology.

C. Transmission Gate Technology Analysis:

i. Like the CMOS implementation, as the technology decreases from 180nm to 32nm while maintaining a constant voltage, the transistor count remains the same.

ii. The average power consumption of the Transmission Gate 4-bit full adder decreases from 0.45µW to 0.07µWas the technology decreases.

iii. The minimum power consumption is observed to be 0.07µW for the 32nm technology.

D. Transistor Count:

i. The CMOS 4-bit full adder contains more transistors compared to the Transmission Gate implementation.

ii. This indicates that the CMOS implementation is bulkier in terms of transistor count.

iii. In summary, the analysis shows that the Transmission Gate implementation of the 1-bit full adder circuit has lower average power consumption compared to the CMOS implementation, regardless of the technology node. Additionally, the Transmission Gate implementation has a lower transistor count, indicating a more compact design.

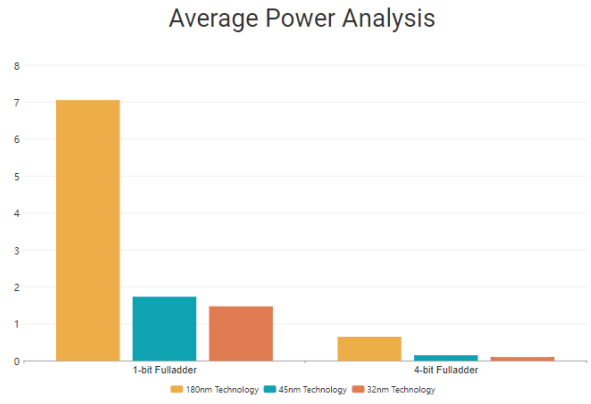


Fig18. Comparison of average power between 1-bit Full adder and 4-bit Full adder of 180nm, 45nm, 32nm technologies using CMOS technology

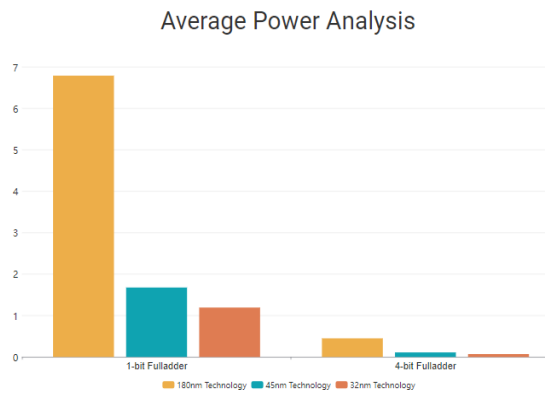


Fig19. Comparison of average power between 1-bit Full adder and 4-bit Full adder of 180nm, 45nm, 32nm technologies using TG technology

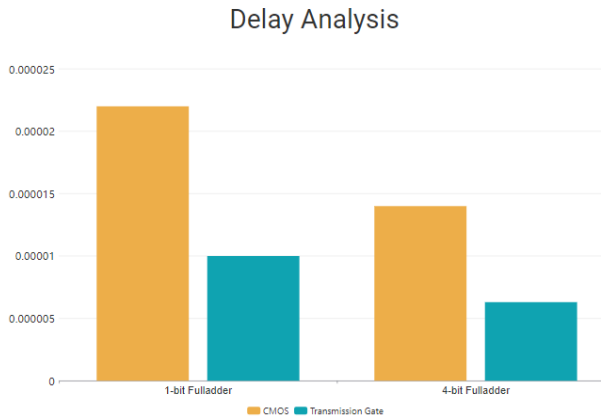


Fig 20. Comparison of delay between 1-bit Full adder and 4-bit Full adder of 180nm, 45nm, 32nm technologies using CMOS and TG technology

In the above figure we found that

i. The average power decreases as the technology decreases.
ii. The 1-bit full adder and 4-bit Full adder are designed using transmission gate has lower average power consumption compared to CMOS for all the technologies.
iii. Number of delays of TG is always less than the number of delays of CMOS.

VI. Conclusion

Low power consumption is a crucial factor in VLSI systems as it contributes to greater reliability. This paper compares and analyzes the performance of 1-Bit full adders and 4-bit Full adder implemented using CMOS and Transmission Gate logic styles across three different technologies: 180nm, 45nm, and 32nm. The analysis focuses on parameters such as average power, supply voltage, and transistor count. The findings reveal that, within each logic style, as the technology node decreases, the average power consumption decreases along with a reduction in the circuit area. This indicates that advancements in technology result in improved power efficiency. Moreover, the study highlights that, for a specific technology node, the transmission gate-based 1-Bit full adder and 4bit Full adder exhibits lower average power consumption, a reduced transistor count, and a smaller area compared to CMOS-based 1-Bit full adder and 4bit Full adder circuits. These results suggest that the transmission gate logic style offers advantages in terms of power efficiency, circuit complexity, and compactness. Overall, the paper emphasizes the importance of low power consumption in VLSI systems and demonstrates the superiority of transmission gate-based 1-Bit full adders in achieving this objective, particularly when compared to CMOS-based counterparts.

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