FPGA Based Pulse Width Modulation

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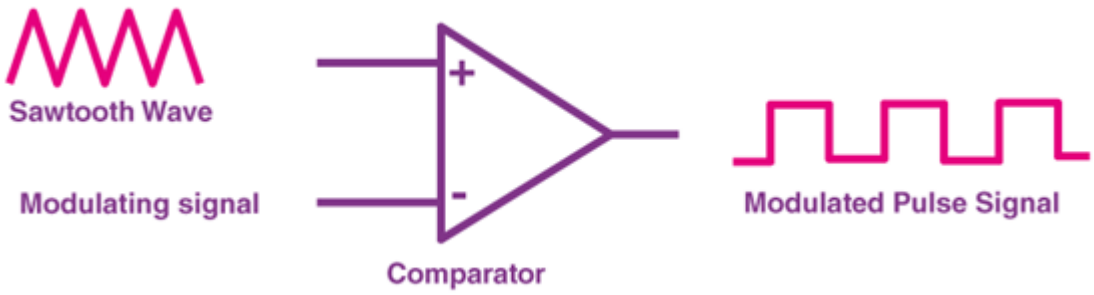
Abstract:

By controlling the voltage applied to different devices, the speed, heat and many parameters can be controlled. There are many methods to control the voltage and one among them is the Pulse Width Modulation technique. The duty cycle ischanged using Pulse Width Modulation. Pulse Width Modulated output can be got by different Circuits. Here, the Pulse Width Modulation block has a register, counter, comparator and RS Latch. The blocks are synthesized using VHDL in QUARTUS-II Integral Development Environment, simulated and downloaded in the Altera FPGA board. The on-time can be changed by changing the register value, the off-time by the counter value. The PWM waveform output is simulated using Modelsim software. Then PWM wave form can beverified by changing the intensity of LED in the FPGA board. In this project, the speed of a DC motor is controlled using the PWM technique. L293D Motor d. In the future, this PWM technique can be used for impedance matching of MPTT to extract maximum power from the Solar Panel.

Introduction:

Pulse width modulation reduces the average power delivered by an electrical signal by converting the signal into discrete parts. In the PWM technique, the signal's energy is distributed through a series of pulses rather than a continuously varying (analogue) signal.

A pulse width modulating signal is generated using a comparator. The modulating signal forms one part of the input to the comparator, while the non-sinusoidal wave or sawtooth wave forms the other part of the input. The comparator compares two signals and generates a PWM signal as its output waveform.



Important Parameters associated with PWM signal:

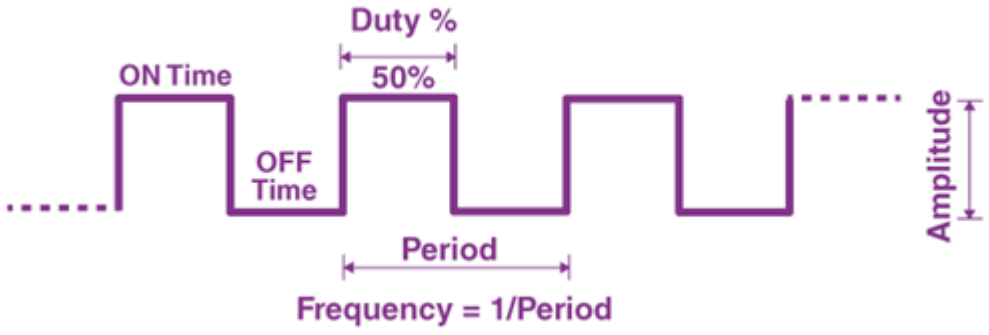
Duty Cycle of PWM:

As we know, a PWM signal stays "*ON*" for a given time and stays "*OFF*" for a certain time. The percentage of time for which the signal remains "*ON*" is known as the duty cycle. If the signal is always "*ON*," then the signal must have a 100 % duty cycle. The formula to calculate the duty cycle is given as follows:

$$DutyCycle = \frac{TurnOnTime}{TurnOnTime + TurnOffTime}$$

The average value of the voltage depends on the duty cycle. As a result, the average value can be varied by controlling the width of the "ON" of a pulse.

Frequency of PWM:



The frequency of PWM determines how fast a PWM completes a period. The frequency of a pulse is shown in the figure above.

The frequency of PWM can be calculated as follows:

Frequency = 1/Time Period
Time Period = On Time + OFF time

Output Voltage of PWM signal

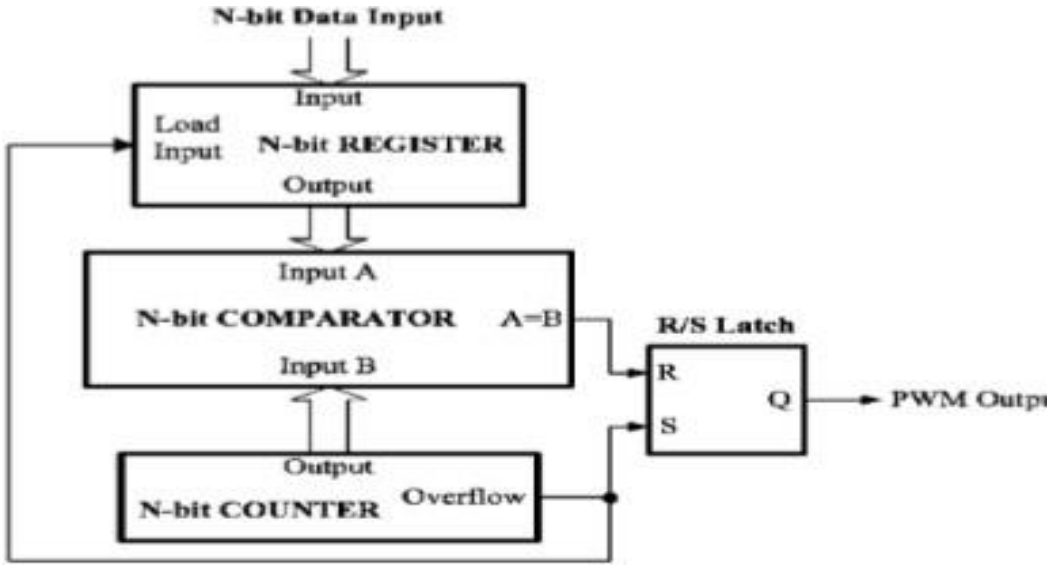
The output voltage of the PWM signal will be the percentage of the duty cycle. For example, for a 100% duty cycle, if the operating voltage is 5V then the output voltage will also be 5V. If the duty cycle is 50%, then the output voltage will be 2.5V.

Types of Pulse Width Modulation Technique

There are three conventional types of pulse width modulation technique and they are named as follows:

- **Trail Edge Modulation –** In this technique, the signal's lead edge is modulated, and the trailing edge is kept fixed.
- **Lead Edge Modulation –** In this technique, the signal's lead edge is fixed, and the trailing edge is modulated.
- **Pulse Centre Two Edge Modulation –** In this technique, the pulse centre is fixed and both edges of the pulse are modulated.

Block Diagram of Pulse Width Modulation :



The system input is an N-bit data word,corresponding to the desired PWM duty cycle value. The register stores the input to be processed. So when load input signal is '1' theregister provides input to output. The counter used is 8 bit up- counter. The N-bit register output containing the N-bit data input is compared with the output value of an N-bit counter by means of a comparator. When these two values become equal the comparator output is used to reset the R/S latch output which produces the PWMwave. The R/S latch output is set when the counter reaches an overflow condition at the end of a PWM period. Also the counter overflow signal is used to load the N-bit data input to the input register. R/S latch is used to set or reset the output. When 'r' signal is '1' output is reset to '0'. When 's' signal is '1' output is set to '1'.The duty cycle of the PWM signal is controlled by the data value.The higher the data value the higher the duty cycle.

Experimental Set up :

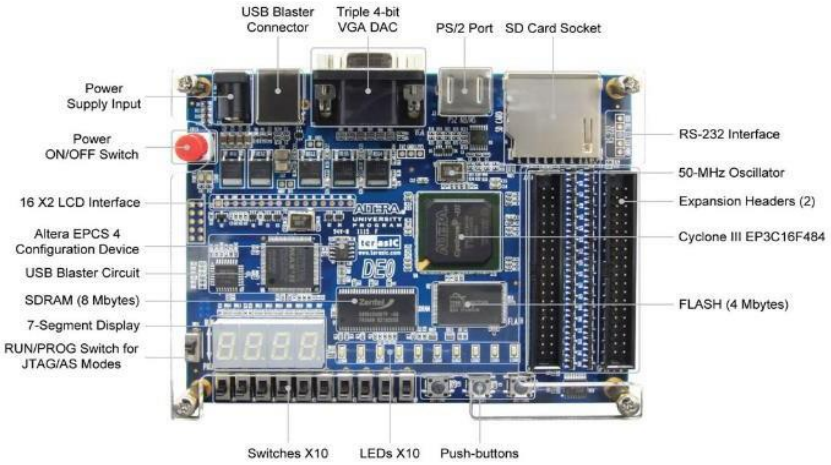


Fig: DE0 Board

DC Motor :

Fig : Brushless DC Motor

The following hardware is provided on the DE0 board:

- Altera Cyclone, III 3C16 FPGA device
- Altera Serial Configuration device – EPCS4
- USB Blaster (on board) for programming and user API control; bothJTAG

and Active Serial (AS) programming modes are supported

- 8-Mbyte SDRAM
- 4-Mbyte Flash memory
- SD Card socket
- 3 pushbutton switches
- 10 toggle switches
- 10 green user LEDs
- 50-MHz oscillator for clock sources
- VGA DAC (4-bit resistor network) with VGA-out connector
- RS-232 transceiver
- PS/2 mouse/keyboard connector
- Two 40-pin Expansion Headers

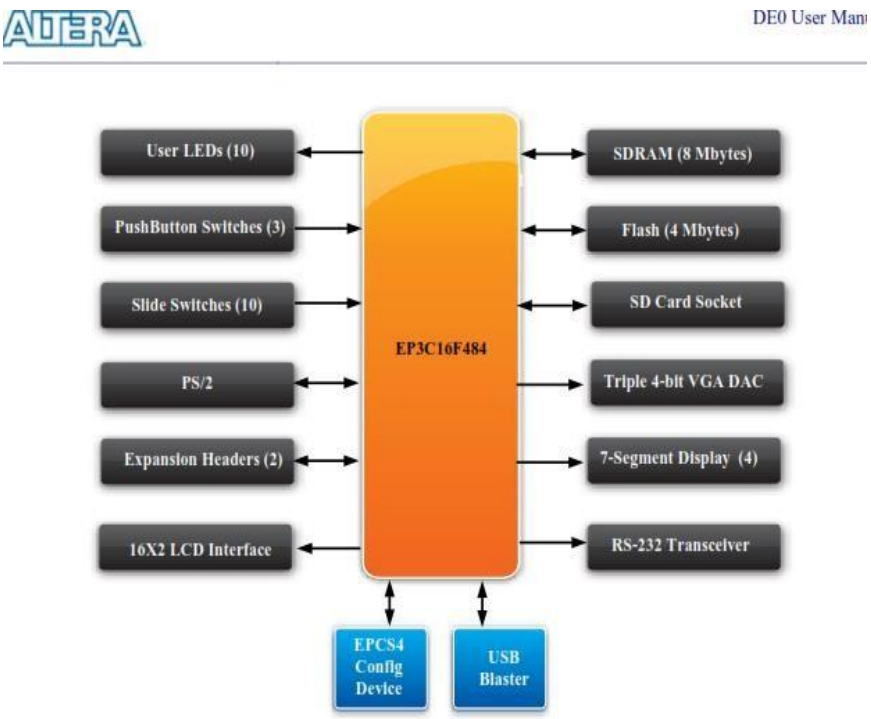


Fig : Cyclone IIII 3C16 FPGA

- 15,408 LEs
- 56 M9K Embedded Memory Blocks
- 504K total RAM bits
- 56 embedded multipliers
- 4 PLLs
- 346 user I/O pins
- FineLine BGA 484-pin package

Built-in USB Blaster circuit:

- On-board USB Blaster for programming and user API (Application programminginterface) control
- Using the Altera EPM240 CPLD

SDRAM

- One **8**-Mbyte Single Data Rate Synchronous Dynamic RAM memory chip
- Supports 16-bits data bus

Flash memory (4-Mbyte NOR Flash memory)

- Support Byte (8-bits)/Word (16-bits) mode

SD card socket to Provide both SPI and SD 1-bit mod SD Card access

Pushbutton switches

- 3 pushbutton switches
- Normally high; generates one active-low pulse when the switch is pressed

Slide switches

- 10 Slide switches
- A switch causes logic 0 when in the DOWN position and logic 1 when in the UP position

General User Interfaces

- 10 Green color LEDs (Active high)
- 4 seven-segment displays (Active low)
- 16x2 LCD Interface (Not include LCD module)

Clock inputs - 50-MHz oscillator

VGA output

- Uses a 4-bit resistor-network DAC
- With 15-pin high-density D-sub connector
- Supports up to 1280x1024 at 60-Hz refresh rate

Serial ports

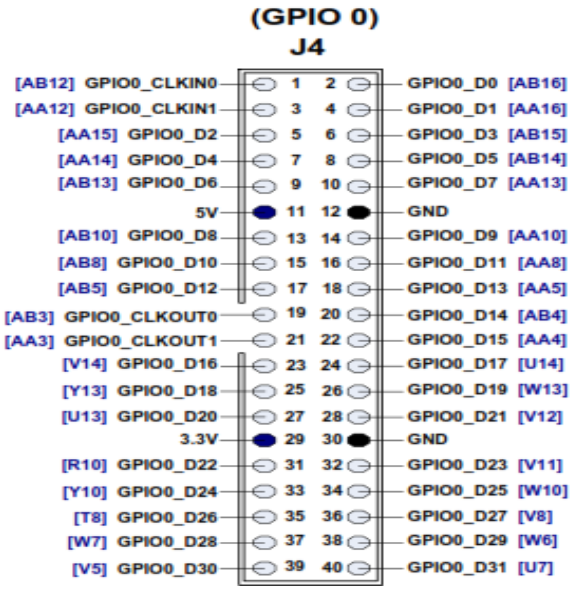
- One RS-232 port (Without DB-9 serial connector)
- One PS/2 port (Can be used through a PS/2 Y Cable to allow you to connect akeyboard and mouse to one port)

Two 40-pin expansion headers

- 72 Cyclone III I/O pins, as well as 8 power and ground lines, are brought out to two40-pin expansion connectors

 40-pin header is designed to accept a standard 40-pin ribbon cable used for IDE hard drives

Expansion Header :



L293D Motor driver:

The l293d is a 16 pin IC, with eight pins, on each side, dedicated to the controlling of a motor. There are 2 INPUT pins, 2 OUTPUT pins, and one ENABLE pin for each motor. L293d consists of two H-bridge H-bridge is the simplest circuit for controlling a low current rated motor.

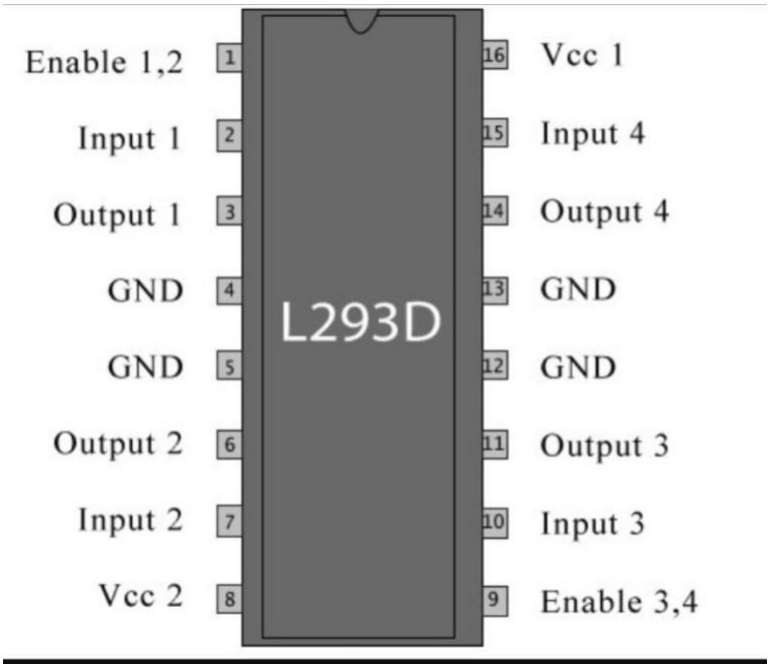
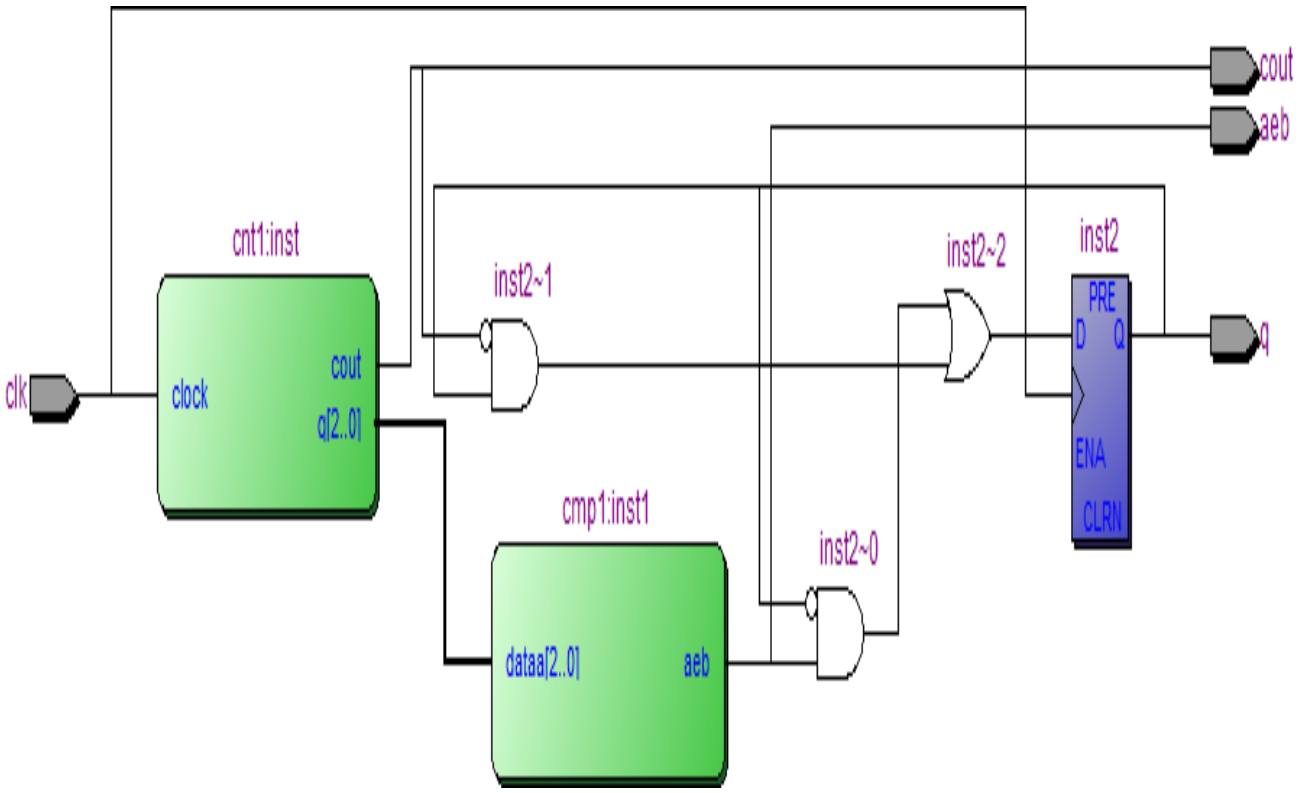


Fig : L293D Motor Driver IC

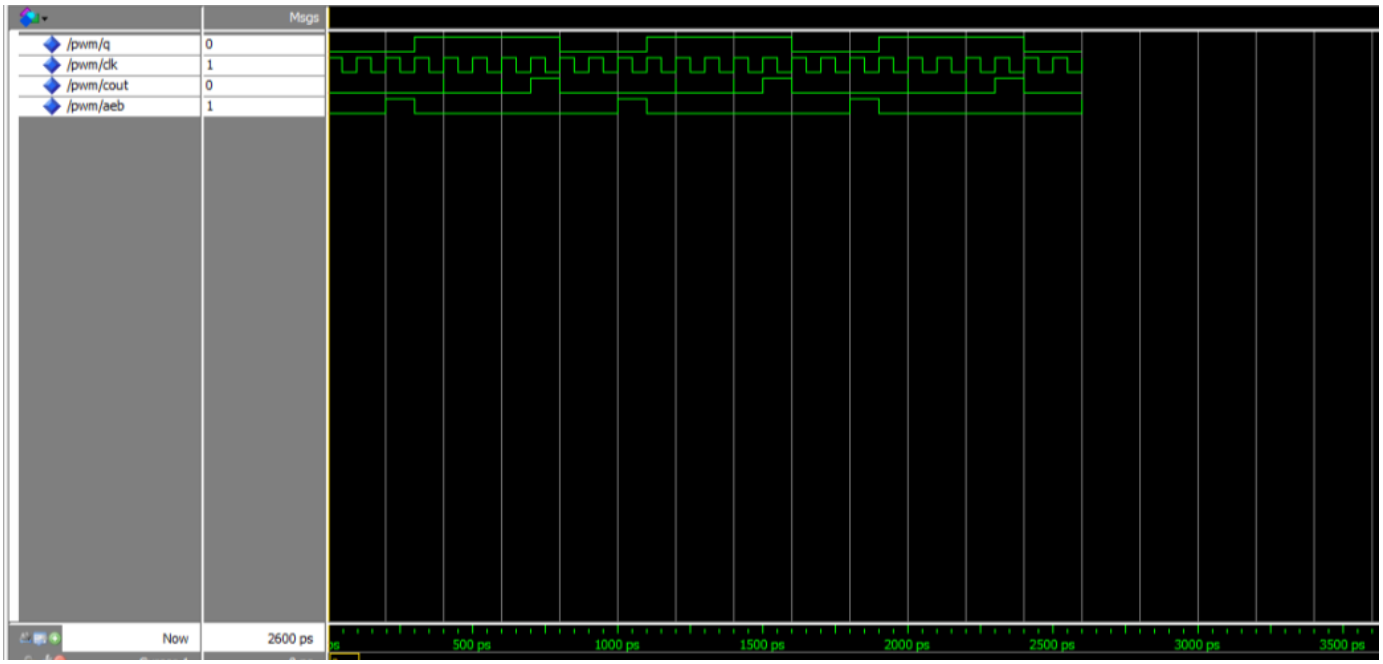
Pin characteristics:

- Enable 1,2 when this is HIGH the left part of the IC will work and whenit is low the left part won't work. So, this is the master control pin for theleft part of IC.
- INPUT 1, when this pin is HIGH the current will flow through OUTPUT 1.
- OUTPUT 1,this pin should be connected to one of the terminal of motor.
- GND, ground pins.
- OUTPUT 2, this pin should be connected to one of the terminal of motor.
- INPUT 2, when this pin is HIGH the current will flow through output 2.
- VC, this is the voltage will be supplied to the motor. So, if you aredriving 12 v DC motors then make sure that this pin is supplied with 12v
- VSS, this is the power source to the IC. So, this pin should be suppliedwith 5v.
- INPUT 4, when this pin is HIGH the current will flow through output 4.
- OUTPUT 4,this pin should be connected to one of the terminal of motor.
- GND, ground pins.
- OUTPUT 3, this pin should be connected to one of the terminal ofmotor.
- INPUT 3, when this pin is HIGH the current will flow through output 3.
- ENABLE 3-4, when this is high the right part of the IC will work and when it is low the right part won't work.so, this is the master control pin for the right part of IC.

Schematic of the PWM Circuit in Quartus – II IDE :



Simulation Result : – Pulse Width Modulation Waveform



Conclusion:

The PWM output got from the circuit drawn using Schematic in Quartus – II IDE was simulated. The functionality is verified. This output is fed to the motor through the motor driver and thus the speed of the input is changed. This work can be extended for the MPPT controller to extract maximum power from the Solar PV panels by adjusting the firing angle in the DC - DC converter used in MPPT.

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