DESIGN AND ANALYSIS OF RESISTIVE MATCH LINE SENSING TECHNIQUE IN TCAM

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Abstract:

Content addressable memory (CAM) is used to replace standard and typical random-access memories (RAM) and set new benchmarks for reliable search operations. Content addressable memories are developed based on the core idea of searching related to content/data. It compares input data with data available in storage memory using parallel comparing techniques. Result is return of addresses of matched data. TCAM are implemented to add one more "don't care" state to the standard CAM's which results in acquiring more content related information comparing to Binary CAM. Performance of content addressable memory depends on storage stability and sensing speed. In CAM, the sensing is carried out through match line. A good ML Sensing technique reduces the ML power consumption also. Simulations are carried out upto 16 bits using cadence 90nm technology and observed that the Resistive ML Sensing has less power consumption and also enhances the voltage drop between match and mismatch states than the Capacitive ML Sensing.

***Keywords: CAM**, RAM, TCAM, ML*

Introduction:

We can't imagine the world without internet. The speed of the internet depends on its search algorithm. However, the search speed of software-based search algorithms is slow. Therefore, high-speed applications use ternary associative memory. For TCAM, the input is the content and the output is the address where the content is stored. The purpose of TCAM designers is to speed up searches and reduce power consumption [1]-[7].

TCAM is a memory element in which the information is stored in rows and search happens in parallel. Content addressable memory, takes content as an input and gives address as an output. If stored data matches with the search data then it gives address in which the data stored. A match or mismatch information is accessed by the sense amplifier. As shown in figure 1, every TCAM cell in a wordline is connected to a common matchline (ML). Initially all matchlines are charged to high voltage. ML value maintains at high voltage if there is a match. Otherwise the respective matchline discharges. To start a new search, all matchlines should be at high voltage. Thus, the frequent charging and discharging happens in content addressable memories. Because of this power dissipation will be more.

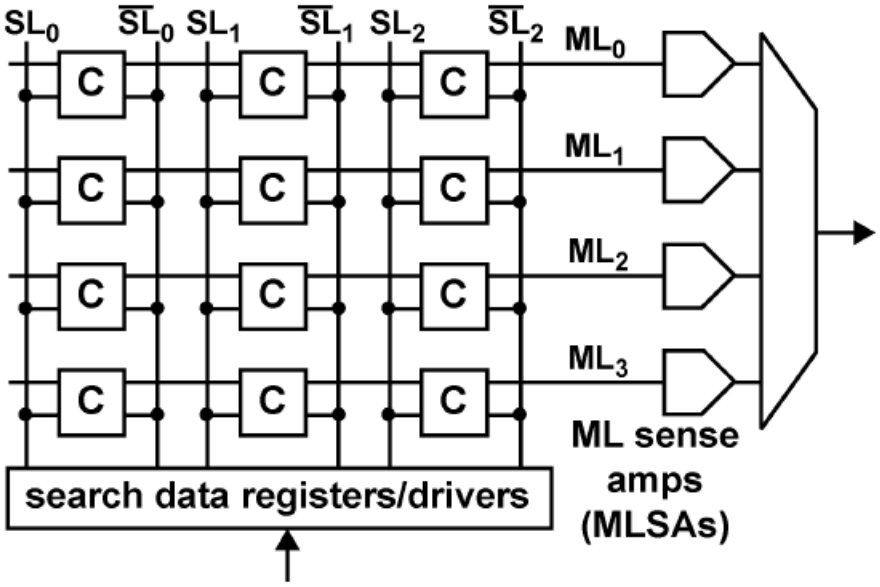


Figure 1: TCAM Architecture

Sensing schemes helps in distinguishing match and mismatch state. Sensing methods helps in reducing power consumption and also to reduce latency of the TCAM. With traditional sensing methods, match linesare usually precharged at high level. In the evaluation phase, only exact matches remain high and mismatched rows remain low. Figure 2 shows a row of TCAM cells with a sensing circuit. Here, ML pre indicates that the Match-Line is precharged, MLSA indicates Match-Line Sensing Amplifier and the TCAM cell used here is NOR type TCAM cell [8].

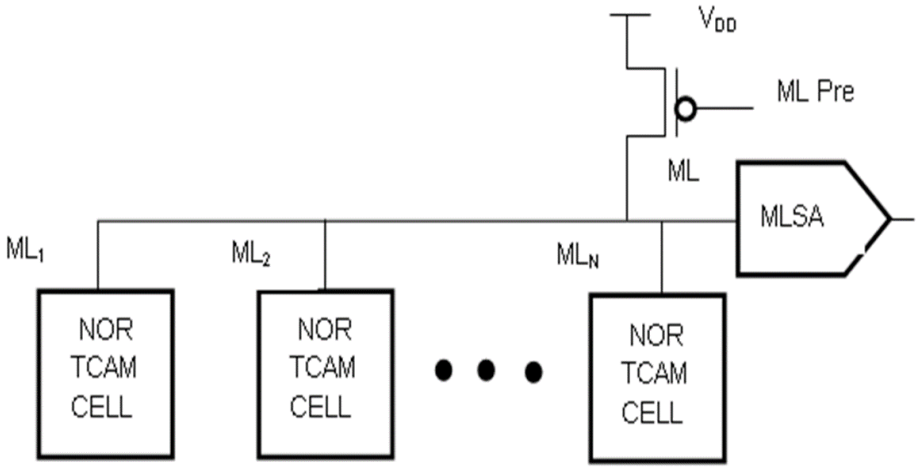
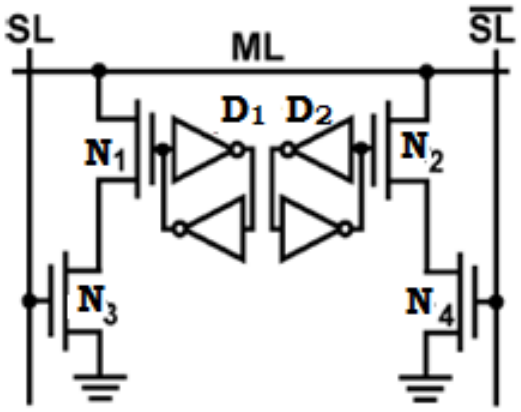


Figure 2: NOR TCAM Architecture

NOR type TCAM cell and its encoding is shown in Figure 3 and Table 1. As TCAM cell has three states hence it requires two SRAM cells. In TCAM, a logic “0” is stored when $D_1 = 0$ and $D_2 = 1$, Logic “1” when $D_1 = 1$ and $D_2 = 0$ and don’t care when $D_1 = 1$ and $D_2 = 1$. In TCAM, a logic “0” is searched when SL = 0 and $\overline{SL} = 1$, Logic “1” when SL = 1 and $\overline{SL} = 0$ and don’t care when SL = 1 and $\overline{SL} = 1$.



Stored Value	Stored	
	D1	D2
0	0	1
1	1	0
X	1	1

Figure 3: NOR -TCAM cell

Table 1: Encoding of NOR cell

Capacitive ML Sensing scheme:

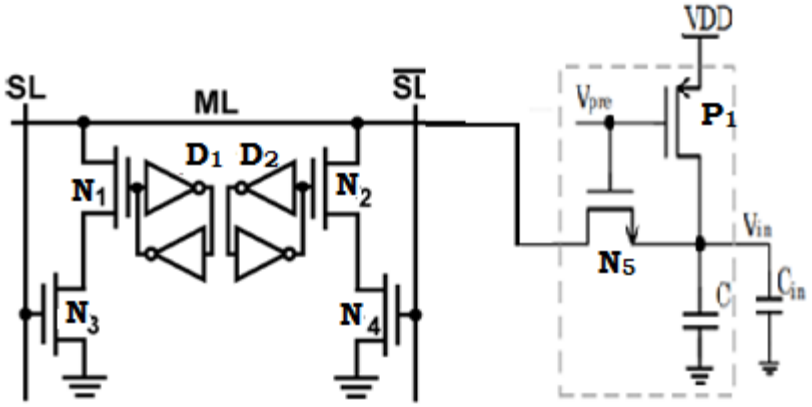


Figure 4: TCAM Cell with Capacitive Sensing Circuit

Figure 4 shows NOR TCAM cell with Capacitive Sensing circuit. Here, a capacitor is used to differentiate between the match and mismatch states. There are two phases in its operation i.e. precharge and evaluation. During precharge phase, N5 transistor is in OFF state and P1 is in ON state so capacitor C is charged to high voltage. Moreover, in precharge phase TCAM cell is not connected to capacitor because of transistor N5.In the evaluation phase, N5 transistor is in ON state and P1 transistor is in OFF state so capacitor C tries to discharge through equivalent resistance of TCAM cell in mismatch condition and in match condition capacitor will not discharge as there is no path for capacitor[9]-13].

Therefore, TCAM cell with a capacitive Sensing circuit enhances the Match-Line voltage in match case but the power consumption is more[14]-[15]. The proposed resistive Match-Line Sensing scheme overcomes the said drawback.

Resistive ML Sensing scheme:

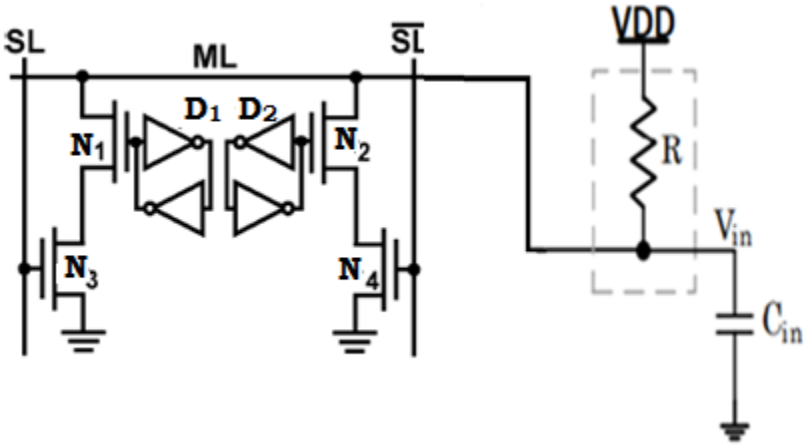


Figure 5: TCAM Cell with Resistive Sensing Circuit

Figure 5 shows the NOR TCAM cell with Resistive Sensing circuit. For every content addressable memory, there are two cases. One is match case and the other one is mismatch case. Search operation in any content addressable memory is done in two phases. In this precharge phase, with the help of precharge transitor ML is charged to high. Where as in the evaluation phase, according to Match-Line voltage it is identified whether it is a match case or a mismatch case. But, In this Resistive Sensing scheme, there is no need for precharge phase. From the Figure 5, it is observed that no precharge transistor is used in this resistive Sensing circuit. In the evaluation phase of the match case, Match-Line remains high and in the mismatch case, Match-Line discharges through the equivalent resistance of the TCAM cells. Resistive Sensing scheme uses a resistor as a voltage divider so the voltage that distinguish the mismatch states and the match state is depict as a voltage divider across the equivalent resistance of the TCAM cells. With the resistive Sensing circuit, the voltage at the Match-Line is enhanced when compared to the other sensing schemes. In mismatch case, Match-Line voltage is reduced at a faster rate when compared to the other sensing schemes.
While comparing Resistive Sensing design with Capacitive Sensing design, Capacitive Sensing uses a pre transistor to precharge its design. Hence, Capacitive Sensing have both precharge phase and Evaluation phase. While, In case of Resistive Sensing only evalution phase is there so that the power consumption is comparatively lower. The speed of resistive sensing design is more compared to capacitive sensing design.

Results:

A NOR type Ternary CAM cell with and withoutMatch-Line Sensing Schemes are also implemented for 1, 2, 4 , 8and 16 bits. All these implementations done on same library filesand attheend power consumptionof the Circuits measured and compared.

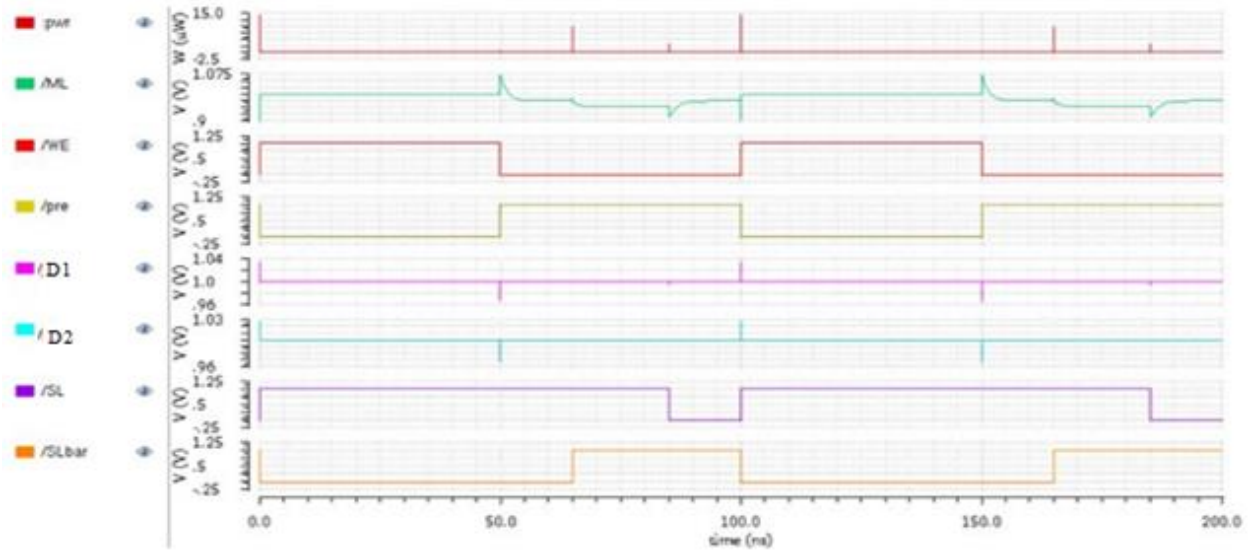


Figure 6.1: Simulated Waveform of 1 Bit Conventional TCAM with logic "X" and search with 0, X, 1

Figure 6.1 shows the simulated waveforms for Conventional TCAM with content D1 =1, D2 =1 i.e., logic "1"and search happens with logic "0", logic "X", and logic "1". From the Figure 6.1 it is observed that it is in match state for entire evaluation phase. The average power consumption here is 72.28 nW.

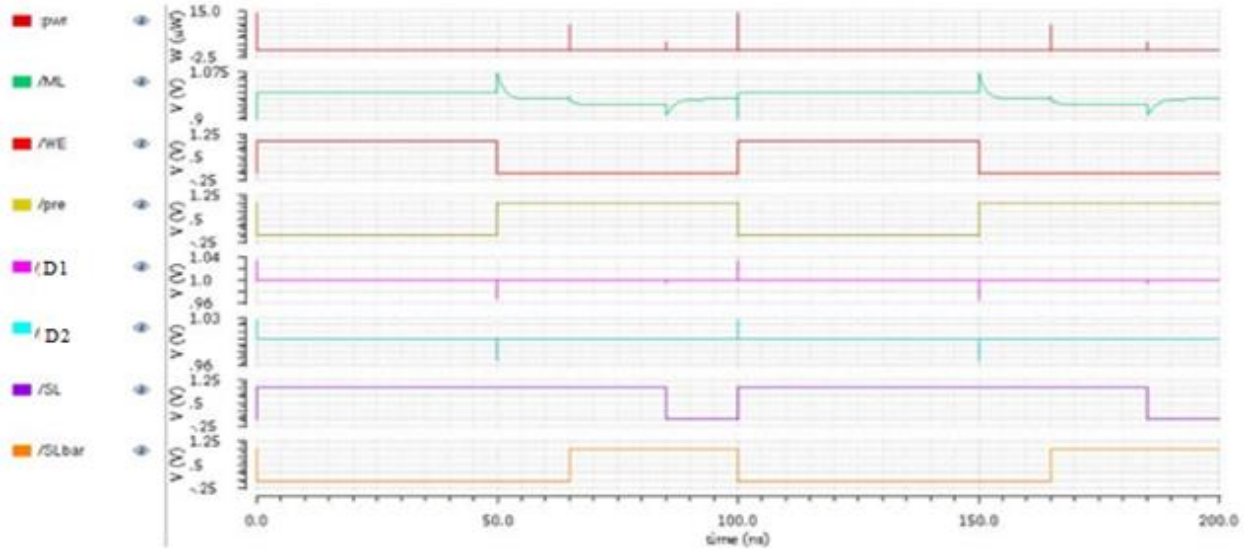


Figure 6.2: Simulated Waveform of 1 Bit TCAM with Resistive Sensing with logic "X" and search with 0, X, 1

Figure 6.2 shows the simulated waveforms for Conventional TCAM with Resistive Sensing Circuit with content D1 =1, D2 =1 i.e., logic "1" and search happens with logic "0", logic "X", and logic "1". From the Figure 6.2 it is observed that it is in match state for search = logic "0" , logic "X" and logic"1". The average power consumption here is 82.30nW.

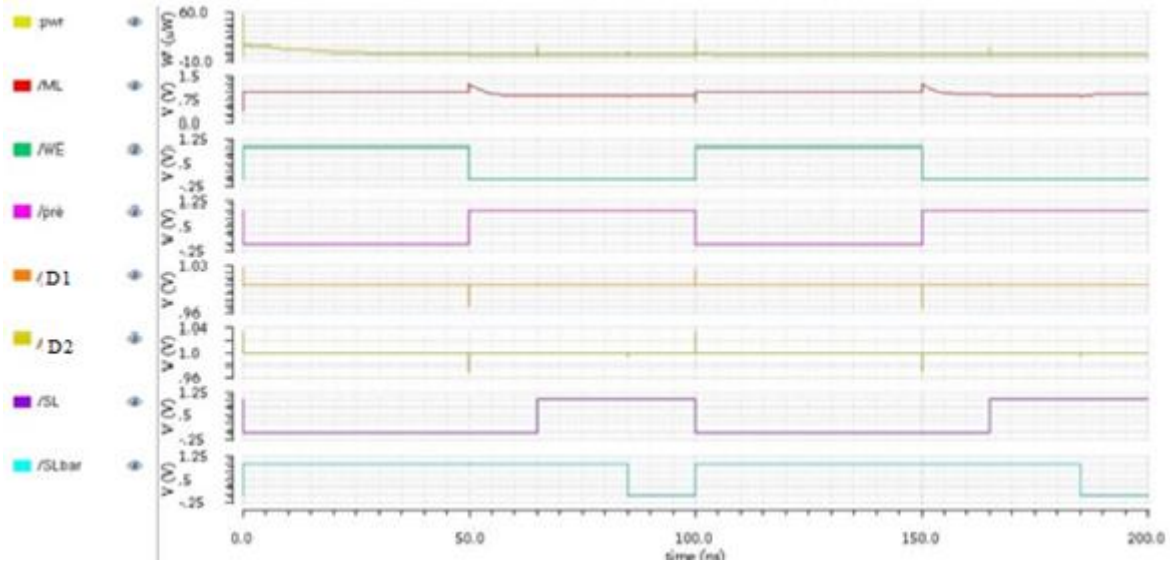


Figure 6.3: Simulated Waveform of 1 Bit TCAM with Capacitive Sensing with logic "X" and search with 0, X, 1

Figure 6.3 shows the simulated waveforms for Conventional TCAM with Capacitive Sensing Circuit with content D1 =1, D2 =1 i.e., logic "1" and search happens with logic "0", logic "X", and logic "1". From the Figure 6.3 it is observed that it is in match state for search = logic "0" , logic "X" and logic "1". The average power consumption here is 982.6nW.

Table 6.1: Comparison of Power Consumption

Stored bits	Search bits	No. of Bits	Power Consumption (µW)		
			NOR TCAM Cell	TCAM with Capacitive ML Sensing	TCAM with Resistive ML Sensing
0	0, X&1	1	11.79	13.22	11.81
1	1, X&0	1	11.79	13.22	11.81
X	0, X&1	1	0.072	0.982	0.082
0	0, X&1	2	22.87	24.17	22.89
1	1, X&0	2	22.87	24.17	22.89
X	0, X&1	2	0.142	1.132	0.161
0	0, X&1	4	44.18	45.43	0.044
1	1, X&0	4	44.18	45.43	0.044
X	0, X&1	4	0.282	1.359	0.315
0	0, X&1	8	84.91	85.28	84.94
1	1, X&0	8	84.91	85.28	84.94
X	0, X&1	8	0.648	1.884	0.698
0	0, X&1	16	161.4	162.9	161.4
1	1, X&0	16	161.4	162.9	161.4
X	0, X&1	16	1.116	2.413	1.717

Table 6.2: Comparison of Match-Line Voltage

No. of bits	ML State	ML Voltage (V)		
		NOR TCAM Cell	TCAM with Capacitive ML Sensing	TCAM with Resistive ML Sensing
1	Match	0.56	0.89	0.90
1	Mismatch	0.35	0.38	0.35
2	Match	0.54	0.84	0.90
2	Mismatch	0.33	0.35	0.33
4	Match	0.52	0.81	0.87
4	Mismatch	0.32	0.32	0.32
8	Match	0.51	0.81	0.86
8	Mismatch	0.30	0.30	0.30
16	Match	0.49	0.76	0.78
16	Mismatch	0.27	0.28	0.27

CONCLUSION

Ternary CAM comes with more features compared with binary CAM. But Ternary CAM is power hungry. Charging and discharging of the matchline not only increases power consumption in TCAM but also effects its speed. By reducing the voltage swing of matchline, the power consumption in TCAM reduced and speed of TCAM also increases.Voltage swing of the matchline is controlled by the matchline sensing techniques. Power consumption in TCAM with conventional Match-Line Sensing techniques and with proposed Match-Line Sensing techniques are compared using Cadence virtuoso 90nm library files and the power reduction in TCAM is observed.

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