Design and Modeling of Binary & M ary Modulation schemes for Virtual Laboratory

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Abstract

The high price of leading-edge equipment required for apprehending digital modulation schemes and their accessibility, especially during the pandemic time, restricts the enrichment of knowledge for most of the students and researchers. Moreover, the design flexibility in hardware implementation is limited. This paper presents an approach for students and researchers to comprehensively study the digital modulation and demodulation process using the free electric circuit simulator LTspice and to compare their performances in both time and frequency domain without using expensive equipment. Circuit design strategy of the modulators and demodulators are also elaborated.

Keywords: *Modulator, M-ary, Transient Analysis, Virtual Lab*

1. Introduction

For a signal to be transmitted to a distance, with tolerable effect of any external interference or noise addition and without getting faded away, it has to undergo a process called Modulation. It improves the Signal to Noise ratio without disturbing the parameters of the original signal. Digital modulation is a process that impresses a digital symbol on to a signal suitable for transmission on a wired or wireless medium in order to receive that signal at the receiving end correctly without any loss of information. Digital modulation provides more information capacity, compatibility with digital data services, higher data security, better quality communications, and quicker system availability. In order to comprehend the concepts of modern communication techniques, the fundamental understanding of digital communication techniques, supported by experiments, is inevitable.

The word binary represents two-bits. In any M-ary system, M corresponds to the number of conditions, levels, or combinations possible for a given number of binary variables (n) where $M=2^n$. M-ary types of digital modulation techniques are used for data transmission in which instead of one-bit, two or more bits are transmitted at a time. More efficient bandwidth utilization can be achieved if the signaling elements contain more than one bit. As a single signal is used for multiple bit transmission, the channel bandwidth is reduced.

In this paper we have elaborated the design and implementation of 4 types of binary modulation techniques. These are Binary Amplitude Shift Keying (BASK), Binary Frequency Shift Keying (BFSK), Binary Phase Shift Keying (BPSK) & Differential Phase Shift Keying

(DPSK). Among M-ary modulation schemes, Quadrature Phase Shift keying (QPSK) modulation technique is the most widely used modulation scheme in modern digital communication systems. It provides high performance on bandwidth efficiency and bit error rate. In this paper we have discussed the design steps of quadrature phase shift keying (QPSK) modulator and demodulator. The performance of all these 5 modulation schemes are compared in both time and frequency domain.

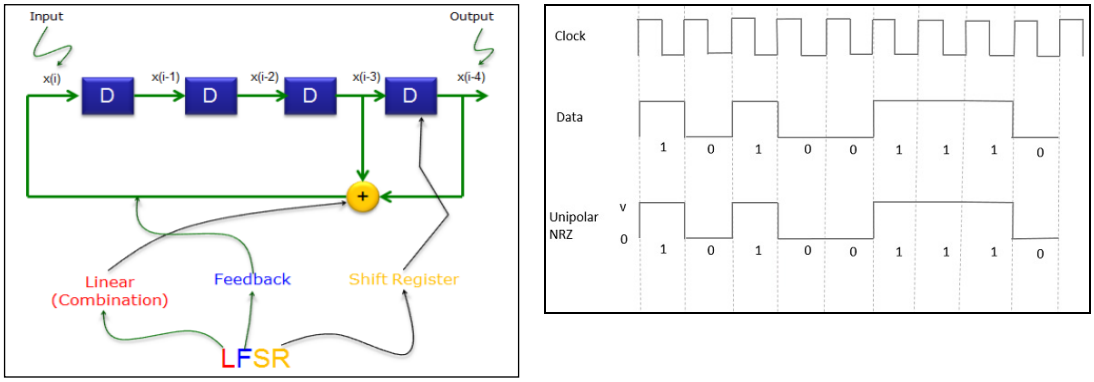
The circuit schematics have been run in the circuit simulator, LTspice. It is a powerful, fast and free simulation software, schematic capture and waveform viewer of analog circuits [1]-[5].Using the software, students can test a possibility of replacing real measurements by results obtained from a simulation. They can reach the relevant conclusions by comparing the results and analyzing the data obtained. Various works have been noted designing analog modulation systems using LTspice [6]. Advanced pulse code modulation system has also been designed using this simulator [7]. In this paper we have proposed the design of a total digital modulation system in a virtual platform which will help the students and researchers to understand, analyze and compare performance of the binary and M-ary modulation system without coming to the laboratory and requiring any hardware implementation.

2. Circuit Modeling

2.1 Generation of Digital Bit Stream

Random sequence is one which consists of 1's and 0's occurring randomly. Linear maximal sequence is a periodic binary sequence which is also called Pseudo Random /Pseudo-noise sequence. The sequence length before repetition is kept long so we can assume that the sequence is truly random. Hence this sequence can be used as a Unipolar Nonreturn to Zero (UPNRZ) bit stream as an input of the Modulation system.

This PN Sequence generator is also known as a Linear Feedback Shift Register (LFSR) which is a shift register circuit where two or more outputs from intermediate steps get linearly combined and feedback to input value.



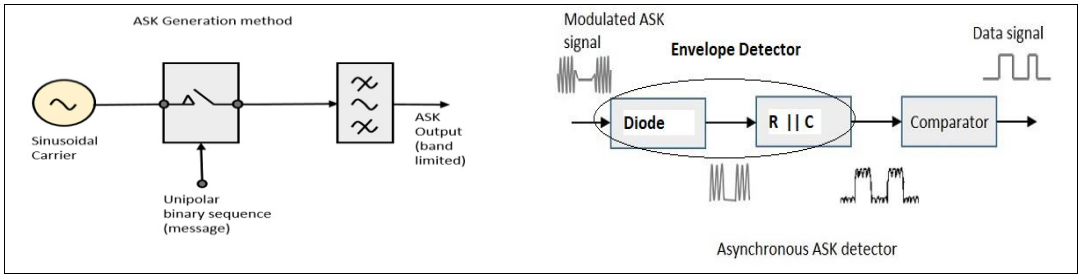
(a) **(b)**

Figure 1. (a) LFSR (Linear Feedback Shift Register) and (b) Generated Data Bit Stream (image collected from web)

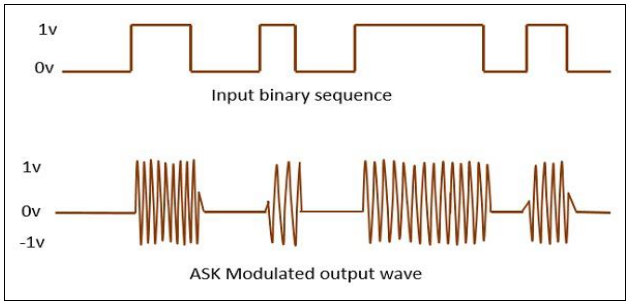
The maximum length of the sequence (L) can be calculated as L = (2N - 1) where N is the number of shift registers. Here, for N = 4, we can get a 15 bit PN Sequence. It is possible from the state transition table of LFSR to generate a predefined sequence [8]

2.2 Binary Amplitude Shift Keying (BASK) Modulator & Demodulator

In ASK (OOK type) a sinusoidal burst of particular amplitude is used to send a binary one and no signal to send a binary zero. The modulator consists of a simple switch whose input is connected to the carrier signal generator and switch operation is controlled by a data stream. An Asynchronous demodulator will be able to recover the data bit. The demodulator circuit consists of an envelope detector followed by a decision device to regenerate the data bit pattern.



(a)

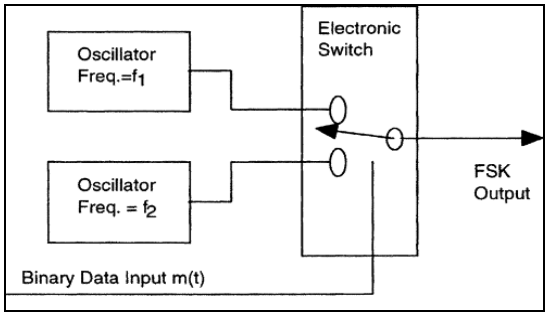


(b)

Figure 2. (a) ASK Modulator & Asynchronous ASK Demodulator (b) ASK Modulated Output (image collected from web)

2.3 Binary Frequency Shift Keying (BFSK) Modulator & Demodulator

In B-FSK modulated wave, bits '1' and '0' are represented by two carrier signals with different frequencies. So the modulator circuit can be implemented using a switch which can select proper input carrier signal frequency depending upon data bit applied at control input of the switch. An Asynchronous receiver will be able to recover the data bit. The band pass filters are designed with pass bands centered about the carrier frequencies to pass the respective modulated signals . Envelope detectors identify the presence of bits. The decision circuit finally decides the bit pattern comparing the outputs of the envelope detector.



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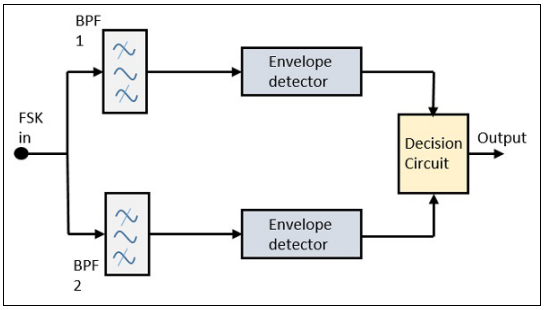

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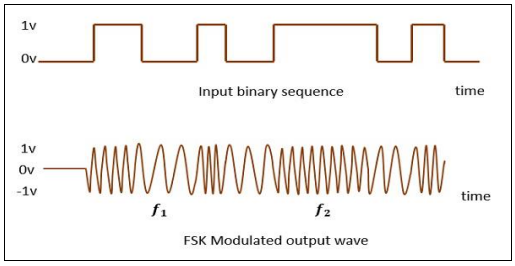
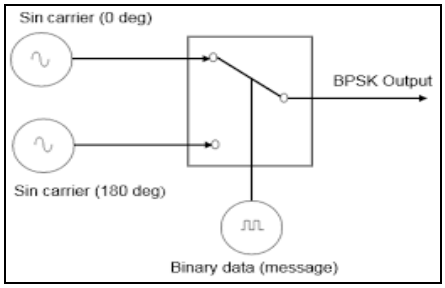


(c)

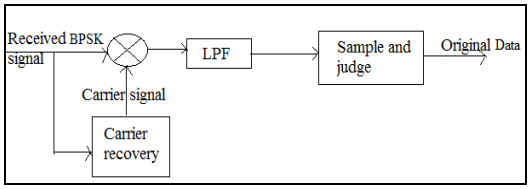
Figure 3. (a) FSK Modulator (b) Asynchronous FSK Demodulator (c) FSK Modulated Output (image collected from web)

2.4 Binary Phase Shift Keying (BPSK) Modulator & Demodulator

In the PSK (phase shift keying) modulation, all transitions of data from 'one' to 'zero' and visiversa, alter the phase of the modulated carrier by 180^o. So we have applied two carriers which are 180^o out of phase at the input of the switch. Depending upon the data bit at control input of the switch, the selected carrier appears at modulated output. In BPSK we have to design a synchronous demodulator since data cannot be recovered through asynchronous demodulation in this modulation scheme. Modulated signals for both one bit and zero bit occupy the same spectral region. So they could not be separated using BPF in an asynchronous demodulator.



(a)



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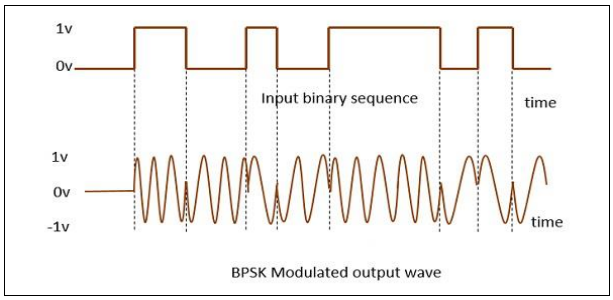


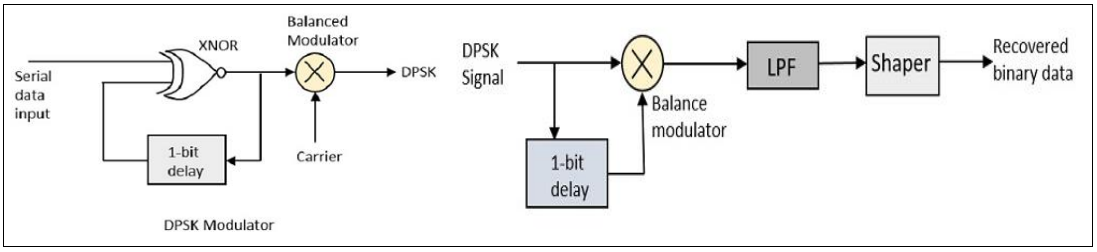
(c)

Figure 4. (a) PSK Modulator (b) Synchronous PSK Demodulator (c) PSK Modulated Output (image collected from web)

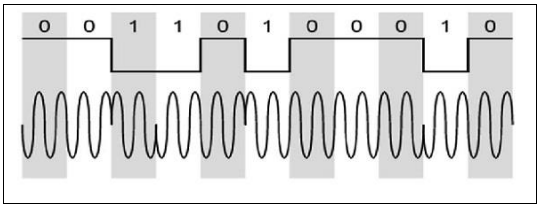
2.5 Differential Phase Shift Keying (DPSK) Modulator & Demodulator

In order to avoid the need to provide synchronous carrier required for detection of BPSK signals, Differential Phase Shift keying (DPSK) scheme is introduced where the binary data is encoded in terms of signal transitions. The encoded data is then used for Phase Shift keying

modulation. Asynchronous receivers are easy and economical to implement from a practical perspective. The differentially encoded bit pattern is applied at input of the modulation system. The demodulation system is asynchronous [9].



(a)

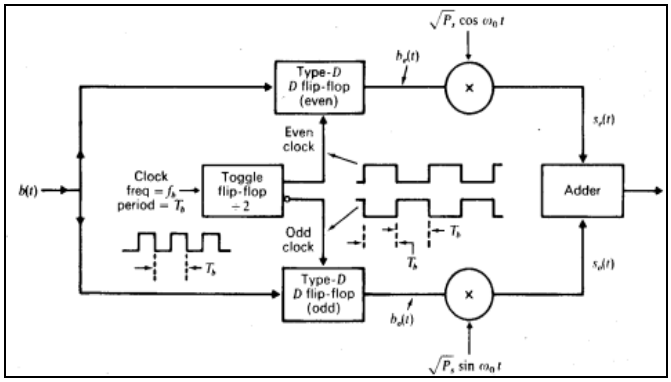


(b)

Figure 5. (a) DPSK Modulator & Asynchronous DPSK Demodulator (b) DPSK Modulated Output (image collected from web)

2.6 Quadrature Phase Shift Keying (QPSK) Modulator & Demodulator

Quadrature Phase Shift Keying (QPSK) is an M ary modulation scheme where M= 4 In this modulation scheme two bits are combined to generate four different symbols which are represented by one of the four possible carriers with phase shifts 0, 90, 180, or 270 degrees modulated at once. QPSK allows the signal to carry twice as much information as ordinary PSK using the same bandwidth [9].



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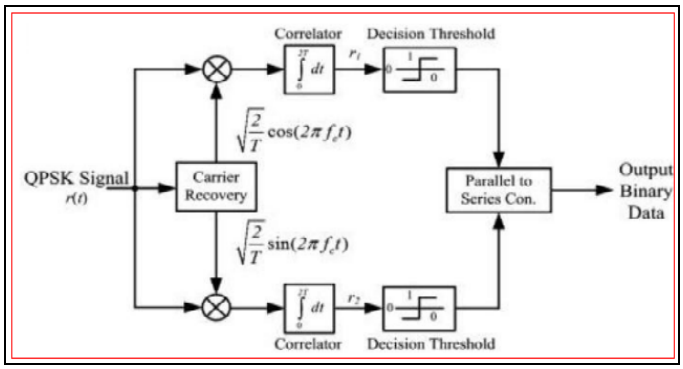

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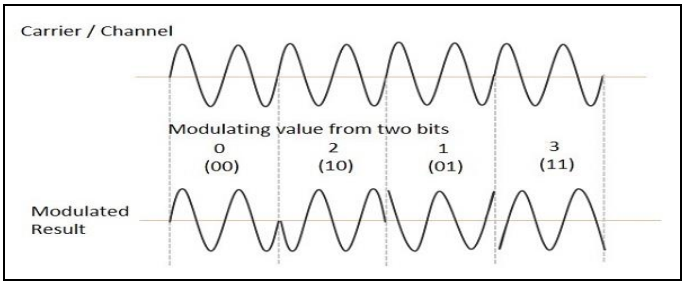


(c)

Figure 6. (a) QPSK Modulator (b) Synchronous QPSK Demodulator (c) QPSK Modulated Output (image collected from web)

3.Circuit Schematics

3.1 Circuit schematic of the 15 bit PN sequence generator

It is shown in Fig.7. In this schematic, a clock with 1 KHz frequency is used to generate bits at 1 Kbps rate [8]. The feedback path from outputs of A3 and A5 ensures maximum length of bit sequence using 4 flip flops. To set the 1st bit of the sequence '1' a 5V trigger is applied at preset inputs of flip flops. The generated bit pattern is used as input data of the digital modulation systems.

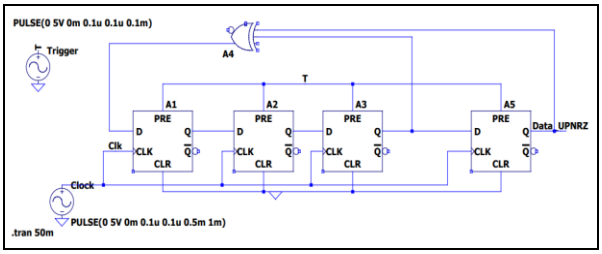


Figure 7. Circuit schematic of PN sequence generator

3.2 The circuit schematic of the BASK modulation system

It is shown in Figure 8. The input of the modulator gets the bit pattern from the PN sequence generator. Modulator circuit is implemented by a simple switch (ADG 1219) which passes the one carrier signal only when input data bit is 1 and other carrier signal when input bit is zero. The asynchronous demodulator circuit is designed using the envelope detector .The R2 & C1 values are calculated using the envelope detector design equation

$$Tc < R2^{*} C1 < Tm$$

where Tc = time period of carrier signal, Tm = time period of message signal. The comparator circuit is made using LT1001.

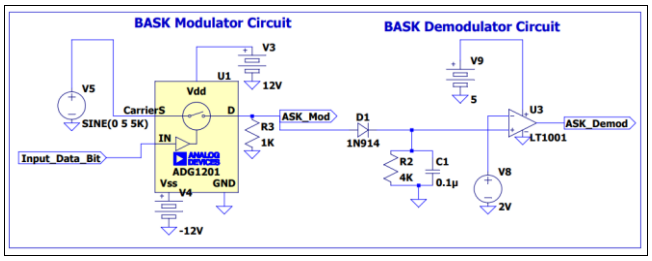


Figure 8. Circuit Schematic of BASK Modulator & Demodulator Circuit

3.3 The circuit schematic of the BFSK modulation system

It is shown in Figure 9. In the modulator circuit, two carrier signals of equal amplitude but with different frequencies are chosen to represent binary '1' and '0'. This circuit is modeled using a simple switch (ADG 1219). In the demodulator circuit the modulated signals are separated using BPFs with suitable bandwidth and centered about the carrier frequencies. Then the envelope detector is used to extract the message bit from the modulated signal. The comparator circuit using OPAMP (LT1001) decides message bits at demodulator output.

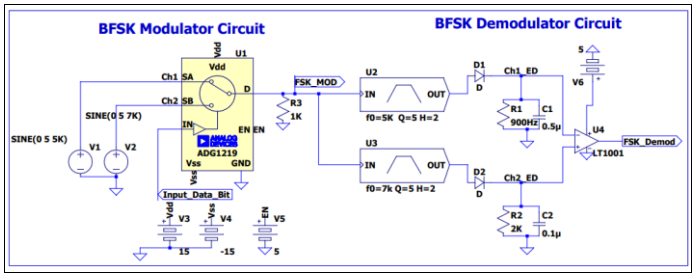


Figure 9. Circuit schematic of BFSK Modulator & Demodulator Circuit

3.4 The circuit schematic of the BPSK modulation system

It is shown in Figure 10. ADG 1219 is used in the modulator circuit. Two sinusoidal carriers of the same frequency but 180 degree out of phase are applied as input signals to switch. So the switch will pass a signal with 0 degree phase for bit 0 and for bit 1 the other signal with 180 degree phase shift. In synchronous demodulator, a behavioral source B1 is used to multiply the received modulated signal with the synchronous carrier. The multiplier output is filtered and the comparator (LT1001) will regenerate the received bit pattern at demodulator output.

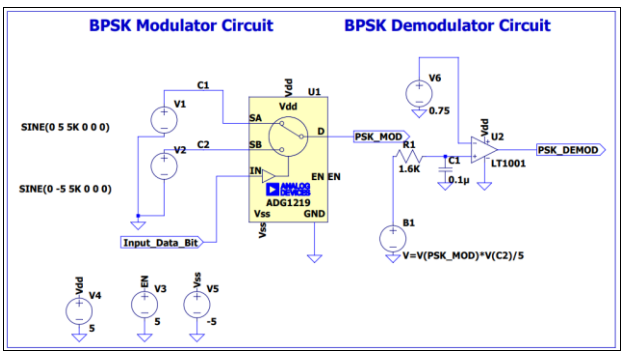
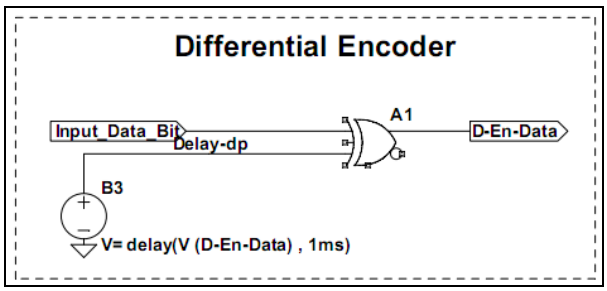


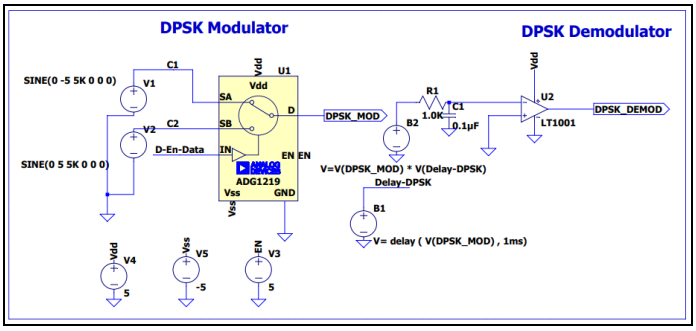
Figure 10. Circuit schematic of BPSK Modulator & Demodulator Circuit

3.5 The circuit schematic of the DPSK modulation system

It is shown in Figure 11. First the differentially encoded data bit is generated as shown in Fig. 11. (a). Then this data bit pattern is applied to the previously designed BPSK modulator. In the asynchronous demodulator section we have used multiplier, LPF and comparator block only.



(a)

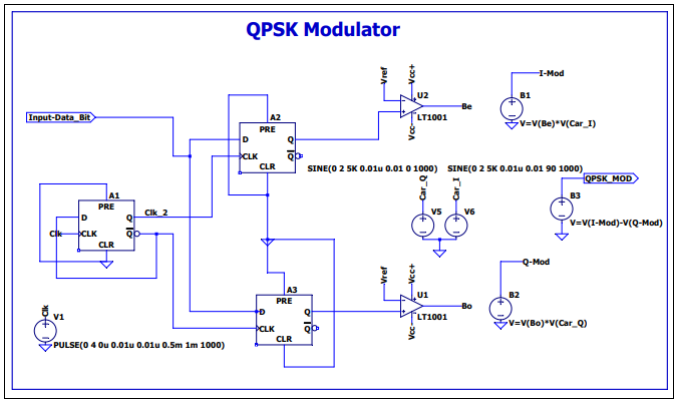


(b)

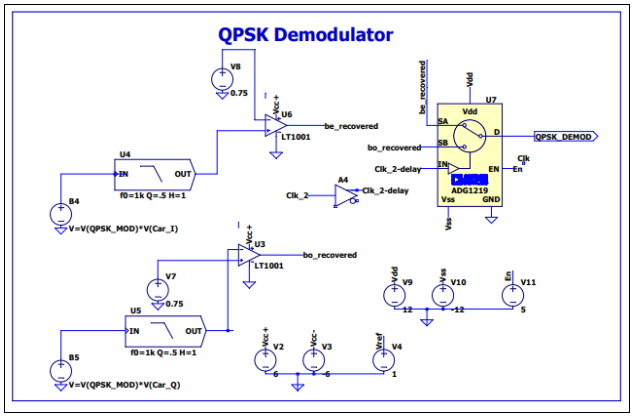
Figure 11. Circuit schematic of (a) Differential Encoder (b) DPSK Modulator - Demodulator Circuit

3.6 The circuit schematic of the QPSK modulation system

It is shown in Figure 12. The serial bit stream is divided in two parallel bit streams containing odd and even bits. Then odd and even bits are modulated simultaneously with quadrature carriers. After adding these two modulated signals we get a QPSK modulated signal as shown in Fig. 12(a). In synchronous demodulator circuits odd and even bits are recovered and converted to serial bit stream at demodulator output.



(a)



(b)

Figure 12. Circuit schematic of (a) QPSK Modulator (b) QPSK Demodulator

The final schematic containing the symbols of all modulation systems is shown in Fig. 13.

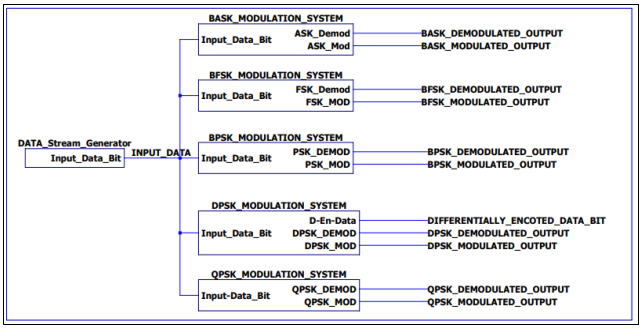


Figure 13. Circuit schematic of Digital Modulation System

4. Results and Discussion

The simulated output in time domain and frequency domain gives us a comparative overview of all these modulation systems. The simulated waveforms in the time domain are shown in Fig. 14. These simulated waveforms are the same as that of theoretically expected ones. It justifies the proper modeling of all the modulation systems in virtual platforms.

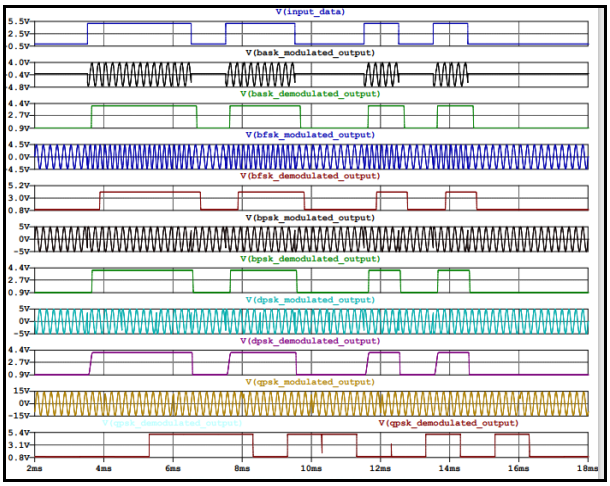


Figure 14. From top to bottom, each plot pane represents the following waveforms in time domain:

a) Input Data Pattern (UPNRZ Sequence)
b) Binary Amplitude Shift Keying (BASK) Modulated output
c) Binary Amplitude Shift Keying (BASK) Demodulated output
d) Binary Frequency Shift Keying (BFSK) Modulated output
e) Binary Frequency Shift Keying (BFSK) Demodulated output
f) Binary Phase Shift Keying (BPSK) Modulated output
g) Binary Phase Shift Keying (BPSK) Demodulated output
h) Differential Phase Shift Keying (DPSK) Modulated output
i) Differential Phase Shift Keying (DPSK) Demodulated output
j) Quadrature Phase Shift Keying (QPSK) Modulated output
k) Quadrature Phase Shift Keying (QPSK) Demodulated output

The simulated waveforms in the frequency domain are shown in Fig. 15.

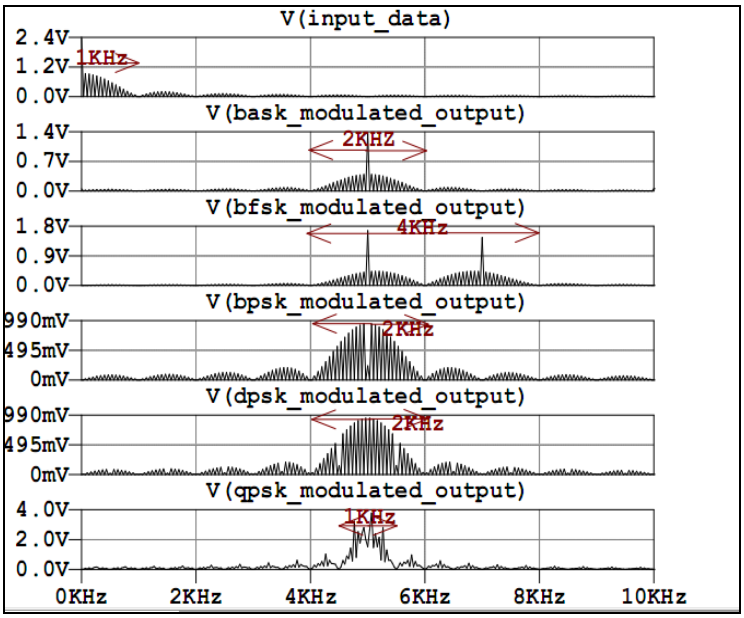


Figure 15. From top to bottom, each plot pane represents the spectral variation of input data and different modulated signals.

a) Input Data Pattern (UPNRZ Sequence)
b) Binary Amplitude Shift Keying (BASK)
c) Binary Frequency Shift Keying (BFSK)
d) Binary Phase Shift Keying (BPSK)
e) Differential Phase Shift Keying (DPSK)
f) Quadrature Phase Shift Keying (QPSK)

From Fig. 15. We can compare the transmission bandwidth requirement and possible transmission bit rate of different digital modulation systems. The comparative table is shown in Table 1.

Table 1. Comparative Study of Different Digital Modulation Systems in Frequency Domain:-

BW of UPNRZ bit stream = fb = 1 KHz

Type of Modulation	Minimum Transmission Bandwidth required
Binary Amplitude Shift Keying (BASK)	B.W. = $2*f_b$ = 2 KHz
Binary Frequency Shift Keying (BFSK)	B.W.= $fc_2 - fc_1 + 2*f_b$ = 7-5+2*1 = 4 KHz
Binary Phase Shift Keying (BPSK)	B.W. = $2*f_b$ = 2 KHz
Differential Phase Shift Keying (DPSK)	B.W. = $2*f_b$ = 2 KHz
Quadrature Phase Shift Keying (QPSK)	B.W. = f_b = 1 KHz

From Table 1 it can be concluded that the QPSK modulation system is the most bandwidth efficient modulation scheme and BFSK is the most bandwidth inefficient scheme. This fact is in perfect accordance with the theoretical estimation of bandwidth of digital modulation systems.

5. Conclusion

LT spice is an efficient circuit simulator which can be used for modeling and simulation of circuits. Thus using this simulator we have designed circuit schematics of various digital modulation and demodulation systems. These schematics can be used as a virtual platform to understand basic characteristics of these schemes. Moreover, we can optimize the system as per our practical requirements, varying the circuit components easily in the virtual platform. We have created a web-based graphic user interface which will provide a platform for students to learn the concepts of digital communication in an interactive way.

Acknowledgement

We acknowledge Dr. Shounak Dasgupta, Associate professor, Electronics & Communication Engineering Department, Heritage Institute of Technology, Kolkata for his valuable contributions in designing the model. We also acknowledge the anonymous creators of the images which we have collected from the web. Use of such images is only for educational purposes, we have no intention to violate copyright norms.

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