Modification over Dithered DPLL to reduce the effect of narrowband channel interference

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Abstract

Digital signal processing based digital phase locked loop (DSP DPLL) are most commonly used for carrier phase tracking in the recent times. Phase locked loop (PLL) behaves in non-linear fashion at the time of signal acquisition. The linearity is restored in the PLL behavior once acquisition is over and signal tracking is taking place. But the same PLL or DSP-DPLL shows non-linearity both during acquisition and tracking when narrowband channel interference is present in the received signal. In this paper, a single tone signal is introduced as channel interference to study the effect on DPLL and its modified versions. To overcome the effect of channel interference, a single tone dither signal is included in the loop of DPLL. Although an improvement in acquisition and tracking performance is observed, but addition of dither signal contributes to the phase error variance and consequently output noise to increase. Therefore, a further modification is proposed by incorporating an additional phase control in the digital control oscillator (DCO) of the loop to improve the output SNR. The proposed loop is implemented on reconfigurable logic platform using System Generator, a tool from Xilinx used to design real time DSP application. The hardware simulation results demonstrate a comparison among traditional DPLL, dithered DPLL and phase controlled dithered DPLL where the proposed version of the loop outperforms others in terms of acquisition and noise rejection.

Keywords

DSP Digital Phase Locked Loop, Phase Controlled DPLL, Channel Interference, Dither DPLL, VHDL System Design, Modified DCO

1. Introduction

Analog or digital forms of Phase locked loop (PLL) are the integral part of various engineering applications [1]. The progress and availability of hardware required for digital signal processing (DSP) are reasons of popularity of DSP based digital phase locked loop (DSP DPLL) [2, 3]. Therefore, digital signal processors are used to implement this carrier locking loop for processing sampled signals [4].

However, carrier locking process includes acquisition and tracking of the received signal where the presence of narrowband channel interference can degrade the DPLL performance in both these modes. The behaviour of the DPLL remains non-linear during tracking and may lead to instability of the loop owing to the interference [5]. To overcome this effect, a single tone signal with low amplitude and high frequency, called dither signal, is introduced at the input of digital control oscillator (DCO) in addition with loop filter output [6]. It helps to improve the acquisition performance of the loop; however, introduction of an additional signal contributes to the increase of noise power and eventually fall in the output SNR.

Therefore, a further modification is incorporated in terms of phase control in the construction of DCO. The input control voltage is able to change the output phase of the DCO along with frequency after this modification [3]. Output noise power can be reduced significantly after addition of this phase control. The following sections elaborate the architecture and theoretical analysis of this loop named as DSP based Phase Controlled Dithered DPLL (PC-Dithered DPLL).

Extreme flexibility of field programmable gate array (FPGA) chips and widespread acceptance of hardware description language (such as VHDL) provides a platform to DSP based system design. Xilinx System Generator, a DSP design tool, runs within Matlab/Simulink environment to develop a methodology of VHDL implementation of real time DSP applications on a reconfigurable logic platform [7, 8]. Here, the proposed loop is designed using these System Generator tools.

2. Model of the Loop

The architecture of the PC-Dithered DPLL is described in the Fig. 1 where all the components are represented in terms of the respective blocks. The in-phase (x_I) and quadrature (x_Q) components are the inputs to the DPLL. The in-phase and quadrature signals from the DCO of the loop along with incoming I-Q signals are used by the phase detector for IQ filtering to avoid the use of an additional RF filter. The noise appearing due to the channel interference is represented at the phase detector output.

A proportional integral (P-I) loop filter is used after the phase detector. The filter response and consequently the loop bandwidth are set by the gains G_1 and G_2 respectively. Thereafter, the DCO estimates the output phase using loop filter output. Two changes are proposed at this point of the loop, a small deterministic phase disturbance in terms of a single tone dither signal is applied to the DCO input in addition with the loop filter output and a provision of changing the output phase along with frequency is incorporated in the DCO. For changing the

output phase, the additional input is called phase modulation (PM) input. The phase estimation reached its desired level with the help of feedback configuration.

3. Theory

The closed loop transfer function of the 2nd order loop can be obtained as [1],

$$H(z) = \frac{G(z)}{1+G(z)} \tag{1}$$

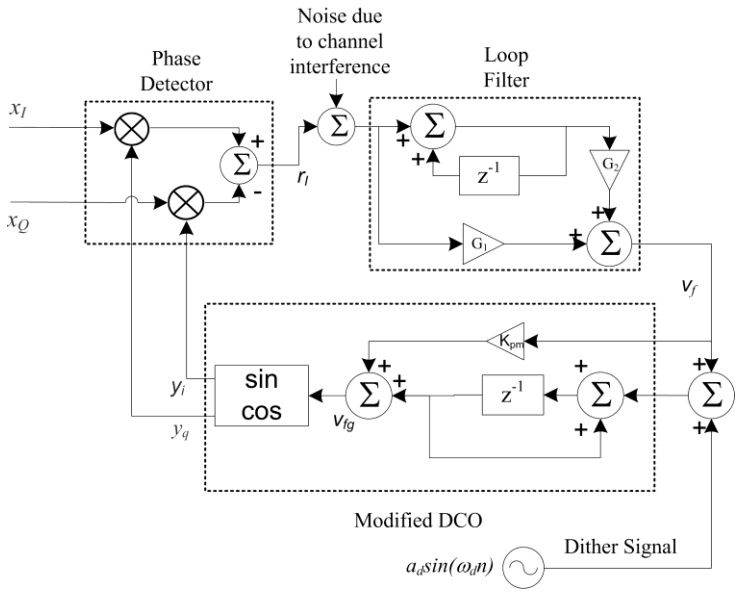

Figure 1. Block diagram of the proposed Dither Loop model

where, G(z), the open loop transfer function is given by,

$$G(z) = D(z)\left(K_{pm} + K_f \frac{z^{-1}}{1-z^{-1}}\right) \tag{2}$$

and

$$D(z) = G_1 + \frac{G_2}{1-z^{-1}} \tag{3}$$

G_1 and G_2 are loop filter coefficients. K_f and K_{pm} are DCO frequency and phase sensitivity respectively.

$H_n(z)$ is the transfer function corresponding to the noise input represented after phase detector and $H_d(z)$ is the transfer function for the response of input dither. These transfer functions are given by,

$$H_n(z) = \frac{1}{1+G(z)} \tag{4}$$

$$H_d(z) = \frac{K_f z^{-1}/(1-z^{-1})}{1+G(z)} \tag{5}$$

Here, $\psi_i(z)$, $N(z)$, $v_d(z)$ are input signal phase, noise and dither signal in Z domain respectively. A is the amplitude of the input signal.

Therefore, phase error and DCO output phase in Z domain can be expressed respectively as follows,

$$\phi(z) = H_n(z)\psi_i(z) - H(z)\frac{n(z)}{A} + H_d(z)v_d(z) \quad (6)$$

$$\psi_o(z) = H(z)\left[\psi_i(z) + \frac{n(z)}{A}\right] - H_d(z)v_d(z) \quad (7)$$

The phase error in time domain can be obtained by taking inverse Z transform of (6) as follows,

$$\phi(k) = h_n(k) * \psi_i(k) - \frac{1}{A}h(k) * n(k) + h_d(k) * v_d(k) \quad (8)$$

The variables $h_n(k)$, $h(k)$ and $h_d(k)$ are inverse Z transform of $H_n(z)$, $H(z)$ and $H_d(z)$ respectively. The noise arising due to the narrowband channel interference is represented by the 2nd term in the right-hand side of (8) which is responsible for the degradation of the tracking performance. The acquisition of the incoming signal is also suffered for the presence of this noise. The response of the dither signal, represented by the 3rd term in R.H.S of (7) can play a major role to improve the phase error response by reducing the effect of this noise arising due to interference. An appropriate choice of dither signal leads to the faster acquisition and better tracking in presence of noise.

When total phase error variances are calculated, it can be expressed as,

$$\sigma_\phi^2 = \sigma_n^2 + \sigma_d^2 \quad (9)$$

where, σ_n^2, σ_d^2 are the variances corresponding to $n(k)$ and $v_d(k)$ respectively.

Although the effect of interference noise is reduced in the phase error, but noise and dither signal contribute towards the unwanted signal power at the output. Therefore, the output SNR is deteriorated. The phase error variance of the loop is also given by [4],

$$\sigma^2 = \frac{N_0 B_L}{P} \quad (10)$$

where, P is representing input signal power, N_0 is single sided power spectral density of the unwanted signal and B_L is the noise bandwidth of the loop. The noise bandwidth is also expressed as [1],

$$2B_L = \frac{B_i}{2\pi j}\oint_C H(z)H(z^{-1})z^{-1}dz \quad (11)$$

When the total phase error variance versus DCO phase sensitivity K_{pm} is plotted in Fig. 2, it clearly represents the improvement of phase error variance when the proportion of phase control is increased in the loop. This is further indicating towards the betterment of output SNR.

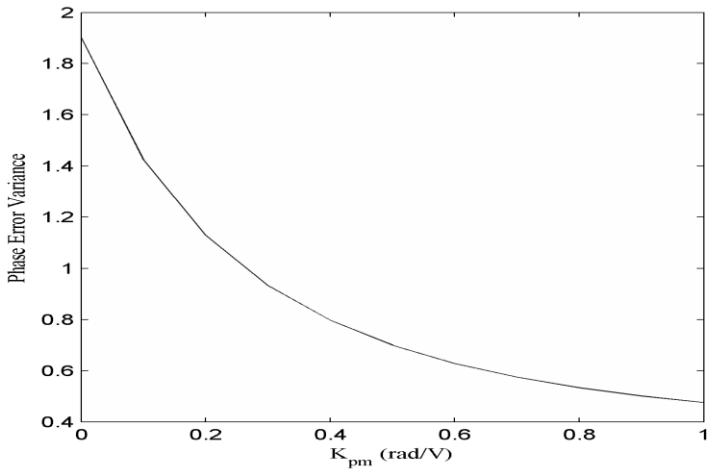

Figure 2. Total phase error variance versus Phase sensitivity K_{pm} (rad/v) when loop filter coefficients $G_1 = 0.2$ and $G_2 = 0.5$ respectively.

4. Hardware Simulation

The simulink block diagram of Fig. 1 is realized using blocks from System Generator, a DSP design tool from Xilinx based on Matlab/Simulink environment, used for the implementation on FPGA platform [7]. The building blocks of DCO in Fig. 1 such as constant, adder, multiplier, unit delay are also available in Xilinx System Generator toolbox. The clock signal and trigonometric function required to built DCO block [6] are found in counter and ROM block respectively. This Xilinx version of DCO is illustrated in Fig. 3.

The similar set of blocks is used to implement the phase detector and loop filter as shown in Fig. 4 and Fig. 5 respectively. Finally, all these sections are connected to build this DSP based PC-dithered DPLL as depicted in Fig. 6. In this model, a single tone signal is connected after transmitter DCO as the channel interference.

The simulation results are obtained and compared for the loop without dither signal, loop with dither signal and loop with dither signal along with additional phase control.

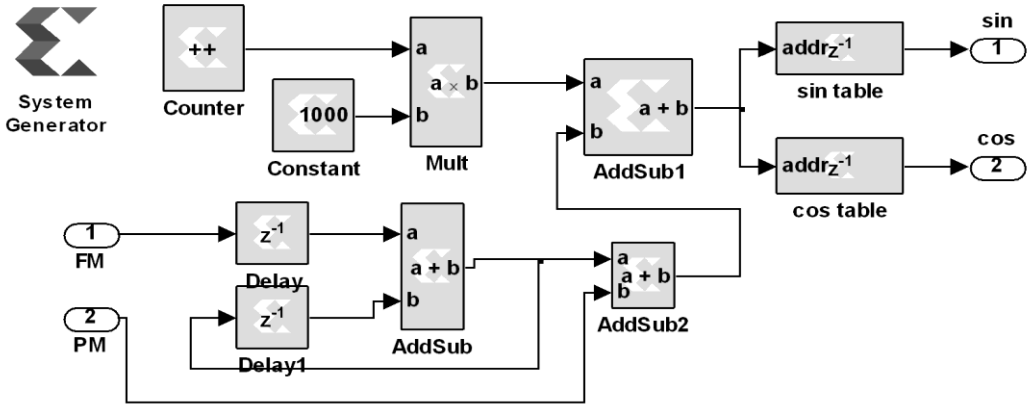

Figure 3. Modified DCO model using Xilinx® system generator simulink® tool.

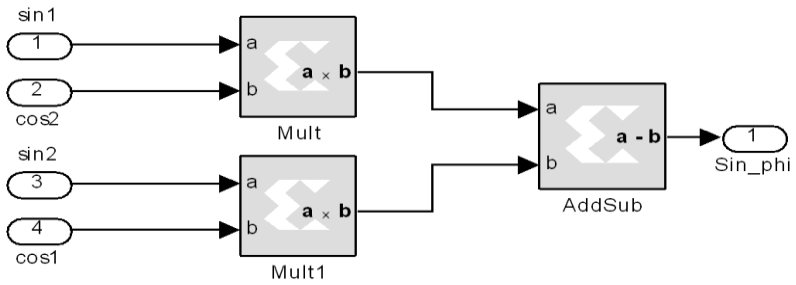

Figure 4. Phase detector model using Xilinx® system generator simulink® tool

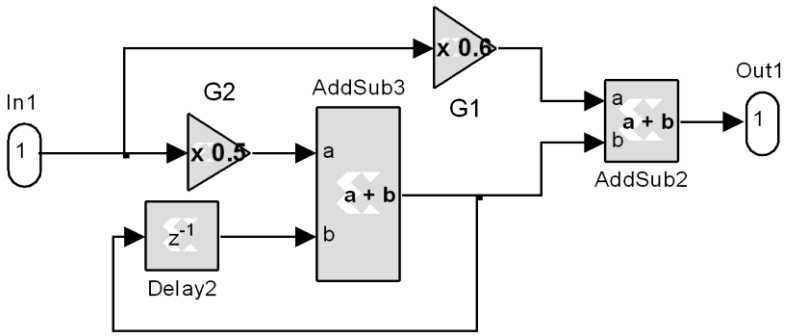

Figure 5. Loop filter model using Xilinx® system generator simulink® tool

5. Simulation Result

Initially, the simulation of the loop (shown in Fig. 6) is carried out to study the acquisition behaviour in absence of interference. The response corresponding to the frequency offset 15Hz is observed for the three loops, traditional DPLL, dithered DPLL and PC-dithered DPLL as shown in Fig.7. It is clearly visible that traditional loop taken longer time (0.43sec) to reach the steady state with respect to dithered loop (0.33sec).

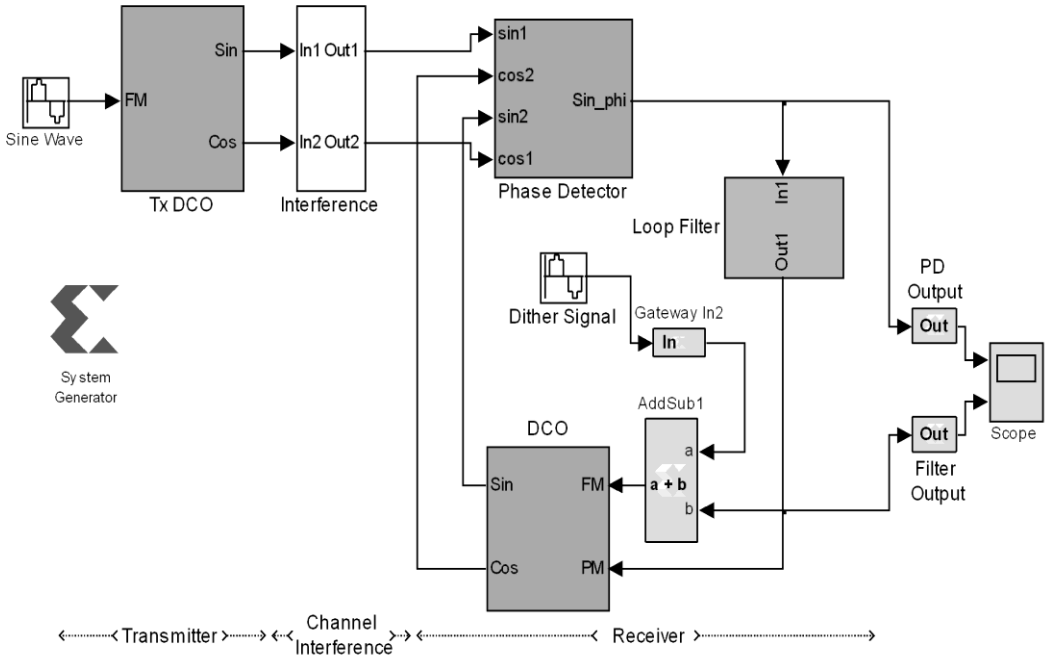

Figure 6: Modulator and proposed Dither Loop model using Xilinx® system generator simulink® tool.

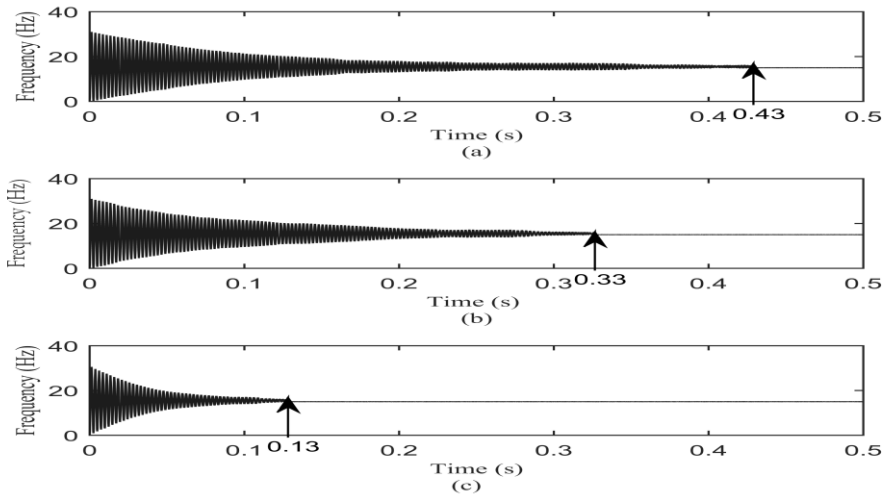

Figure 7. Transient response curves of (a) DPLL, (b) Dithered DPLL, (c) PC Dithered DPLL when input frequency offset is 15 Hz.

However, after application of phase control the same dithered loop settles even earlier (0.13sec).To study the tracking behaviour of the loop a multi-tone FM signal is used where tone signal frequencies are 60Hz, 100Hz and 180Hz respectively. A single tone signal with frequency 200Hz and amplitude 1/10th of the message signal is introduced as channel interference. One sided amplitude spectra of the demodulated signal by the three versions of the loop are presented in Fig. 8. Once again traditional loop fails to track the incoming signal where as dithered loop is able to track successfully. But noise appearing in the spectrum due to interference reduced significantly when phase control is introduced in the loop.

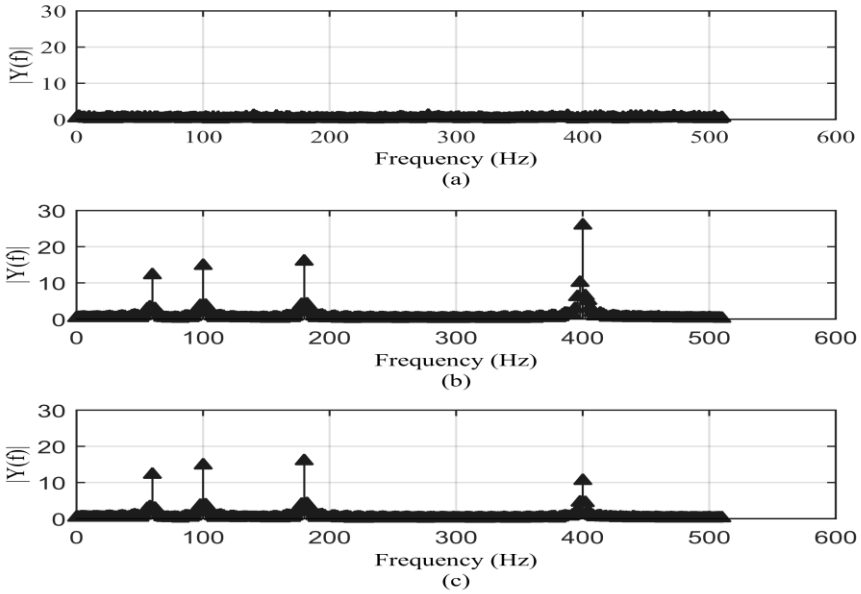

Figure 8. One sided amplitude spectrum of demodulated output of (a) DPLL, (b) Dithered DPLL, (c) PC Dithered DPLL for a multi-tone (60Hz, 100Hz and 180Hz) modulated input FM in presence of narrowband channel interference.

6. Conclusion

The architecture of a modified version of dithered DPLL has been demonstrated. The proposed modification has been analyzed theoretically in support of noise reduction. The implementation of the proposed loop on a platform supported by VHDL is the validation the proposed design. Hardware simulation results have been presented to prove the performance enhancement of the proposed loop as promised theoretically.

7. References

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